UNDERSTANDING COMPUTE EXPRESS LINK 2.0: A CACHE-COHERENT INTERCONNECT

Jim Pappas, Chairman

CXL Consortium
Industry trends are driving demand for faster data processing and next-generation data center performance.
CXL CONSORTIUM

CXL Board of Directors

Industry Open Standard for High Speed Communications

150+ Member Companies
CXL DELIVERS THE RIGHT FEATURES AND ARCHITECTURE

**Challenges**
- Industry trends driving demand for faster data processing and next-gen data center performance
- Increasing demand for heterogeneous computing and server disaggregation
- Need for increased memory capacity and bandwidth
- Lack of open industry standard to address next-gen interconnect challenges

**CXL**
An open industry-supported cache-coherent interconnect for processors, memory expansion and accelerators

**Coherent Interface**
Leverages PCIe with 3 mix-and-match protocols

**Low Latency**
- Cache and Memory targeted at near CPU cache coherent latency

**Asymmetric Complexity**
Eases burdens of cache coherent interface designs

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REPRESENTATIVE CXL USAGES

Caching Devices / Accelerators
- Processor
- DDR
- Memory Buffers
- Accelerator NC
- Cache
- PROTOCOLS: CXL.io, CXL.cache
- USAGES: PGAS NIC, NIC atomics

Accelerators with Memory
- Processor
- DDR
- Memory Buffers
- Accelerator
- Cache
- PROTOCOLS: CXL.io, CXL.cache, CXL.memory
- USAGES: GP GPU, Dense computation

Memory Buffers
- Processor
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- PROTOCOLS: CXL.io, CXL.memory
- USAGES: Memory BW expansion, Memory capacity expansion, Storage class memory
THE NEW FEATURES OF CXL 2.0
DATA CENTER: LOOKING OUTSIDE IN: SCOPE OF CXL 2.0 OVER CXL 1.1

CXL 1.1 – single Node PCIe and CPU-CPU Coherency interconnect

Memory/Accelerator Pooling with Single Logical Devices

Memory Pooling with Multiple Logical Devices

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# CXL 2.0 Scope: Hot-Plug, Persistence, Switching, and Dis-aggregation

<table>
<thead>
<tr>
<th>Feature</th>
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<tbody>
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<td>CXL PCIe End-Point</td>
<td>CXL device to be discovered as PCIe Endpoint. Support of CXL 1.1 devices directly connected to Root-Port or Downstream Switch Port.</td>
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CXL 2.0 is fully backwards compatible with CXL 1.0/1.1 (see next slide for details). CXL 2.0 spec Rev 0.7 in Q1, 2020; Rev 0.9 in Q2, 2020, and CXL 2.0 in Q3, 2020. Predictable spec release cadence by CXL consortium to help the ecosystem plan better.
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BENEFIT OF CXL 2.0 SWITCHING
Pooling

Memory/Accelerator Pooling with Single Logical Devices

CXL 2.0 Switch

D1 | D2 | D3 | D4 | D#

H1 | H2 | H3 | H4 | H#

Memory Pooling with Multiple Logical Devices

CXL 2.0 Switch

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BENEFITS OF CXL 2.0
and Persistent Memory

Moves Persistent Memory from Controller to CXL

Enables Standardized Management of the Memory and Interface

Supports a Wide Variety of Industry Form Factors

CPU
DRAM CXL 1.1/1.0
CXL 2.0
Persistent Memory
Performance SSD
Capacity SSD
HDD

Latency: nanoseconds

DRAM CXL 1.1/1.0
CXL + PM Fills the Gap!

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CXL 2.0 provides Integrity and Data Encryption of traffic across all entities (Root Complex, Switch, Device)
## CXL 2.0: BACKWARDS COMPATIBLE WITH CXL 1.0/1.1

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<tr>
<th>CPU – Device Connectivity</th>
<th>CXL 1.X (1.1/1.0) EP</th>
<th>CXL 2.0 EP</th>
<th>PCIe EP/ Switch</th>
<th>Comments</th>
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<tr>
<td>CPU with CXL 1.x</td>
<td>CXL 1.x</td>
<td>CXL 1.x</td>
<td>PCIe</td>
<td>CXL 2.0 EP needs to support both RCiEP and EP modes</td>
</tr>
<tr>
<td>CPU with CXL 2.0</td>
<td>CXL 1.x</td>
<td>CXL 2.0</td>
<td>PCIe</td>
<td>CXL 2.0 CPU also needs to be bi-modal for backwards compatibility</td>
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<th>CXL 2.0 Switch Connectivity</th>
<th>Operation</th>
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<td>Upstream: CPU</td>
<td>Only CXL 2.0</td>
<td>Since switch definition is with CXL 2.0, the platform requirement is upstream port be a CXL 2.0 CPU</td>
</tr>
<tr>
<td>Downstream: CXL Device</td>
<td>CXL 1.x or CXL 2.0</td>
<td>All downstream CXL ports work as CXL 1.x or CXL 2.0 – mix and match to the device's capability</td>
</tr>
<tr>
<td>Downstream: PCIe EP/ Switch</td>
<td>PCIe</td>
<td>Any CXL switch downstream Port must be able to support a PCIe hierarchy, either an EP or a PCIe switch but assigned to <em>one</em> domain</td>
</tr>
<tr>
<td>Downstream: CXL Switch</td>
<td>N/A</td>
<td>CXL 2.0 is defined only as a single level switch for multiple virtual hierarchies (no cascading of CXL switches)</td>
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IN SUMMARY

**CXL Consortium momentum continues to grow**
- 150+ members and growing
- Responding to industry needs and challenges

**CXL 2.0 introduces new features & usage models**
- Switching, pooling, persistent memory support, security
- Fully backward compatible with CXL 1.1 and 1.0
- Built in Compliance & Interop program

**Call to action**
- Join CXL Consortium
- Visit [www.computeexpresslink.org](http://www.computeexpresslink.org) for more information
- Follow us on [Twitter](https://twitter.com) and [LinkedIn](https://www.linkedin.com) for more updates!
THANK YOU
Jim Pappas, CXL Chairman
CXL Consortium