



2023 OFA Virtual Workshop

# UNIVERSAL CHIPLLET INTERCONNECT EXPRESS™ (UCIE™): BUILDING AN OPEN ECOSYSTEM OF CHIPLETS FOR ON-PACKAGE INNOVATIONS

Keynote by:

Dr. Debendra Das Sharma

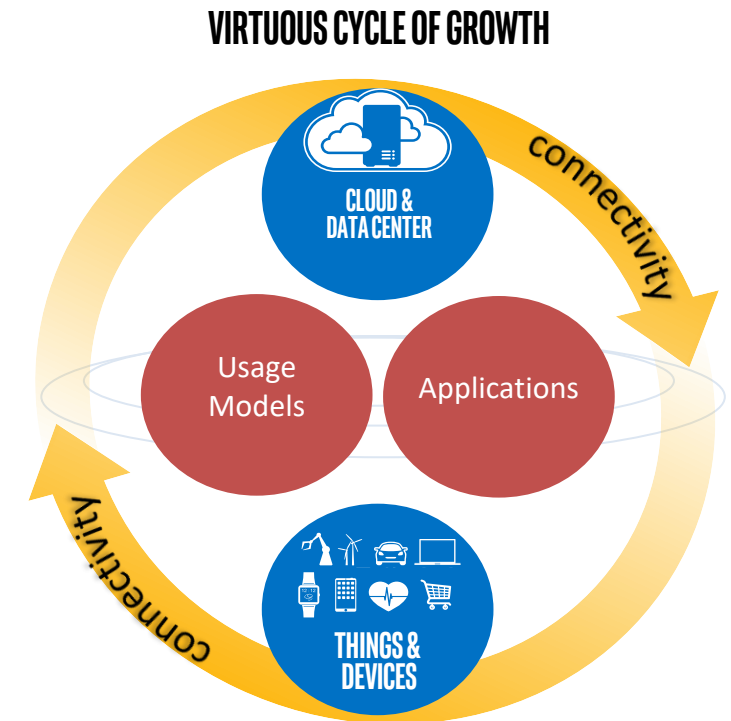
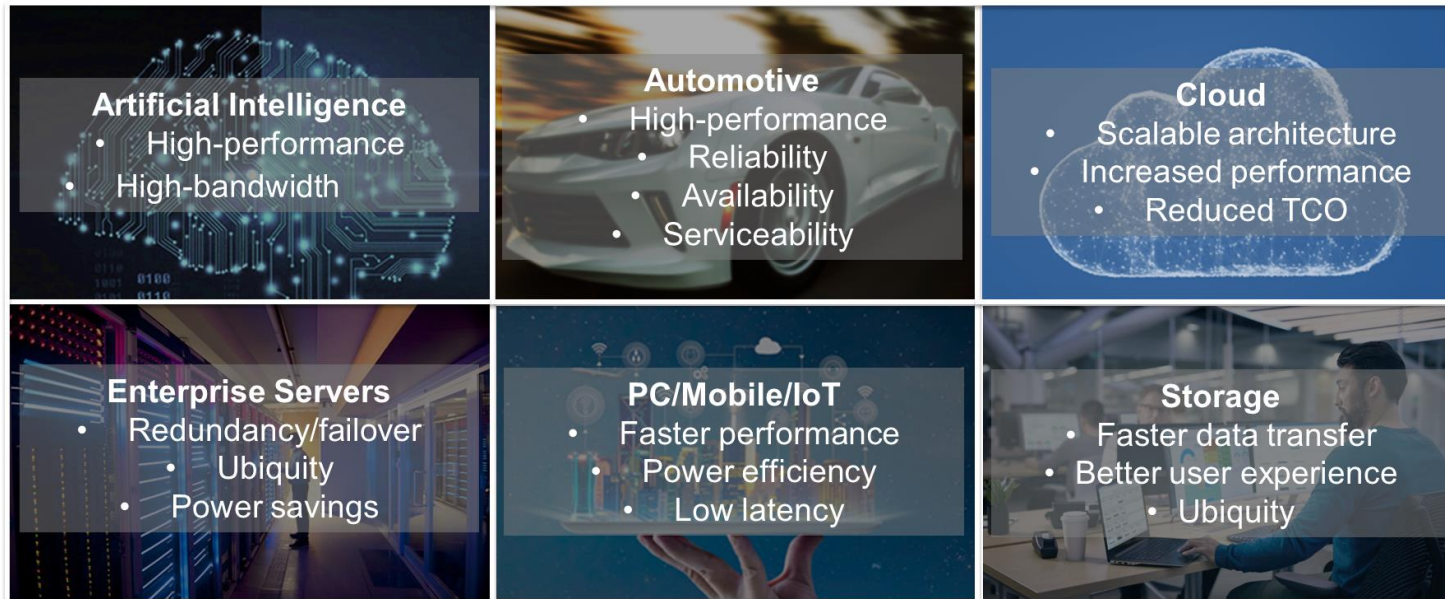
Chair, UCle Consortium

Intel Senior Fellow and co-GM Memory and I/O Technologies, Intel Corporation

# AGENDA

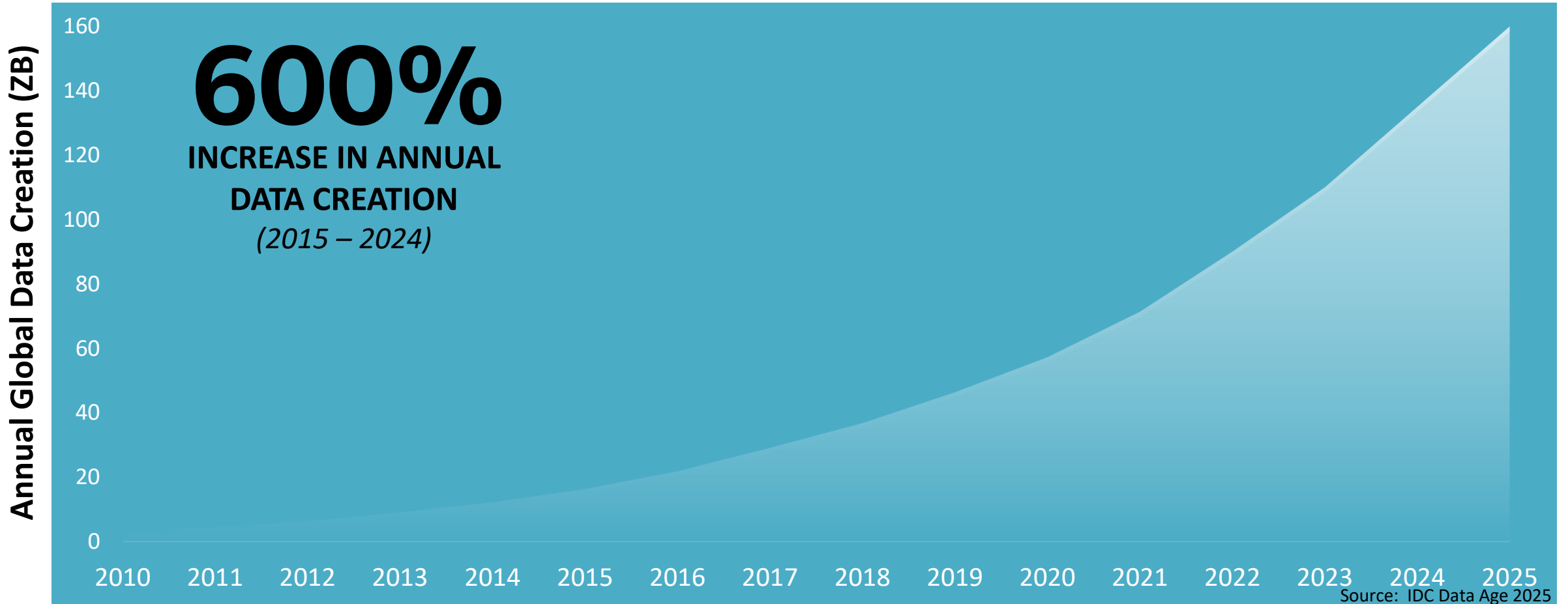
- **Mega-Trends in compute landscape**
- **Interconnects and Fabrics - an important pillar of compute**
- **On-Package Interconnects: Opportunities and Challenges**
- **Universal Chiplet Interconnect Express (UCIe): An Open Standard for Chiplets**
- **Future Directions**

# MEGA-TRENDS IN THE COMPUTE LANDSCAPE



- **Insatiable demand for compute, storage, and data movement**
- **Innovative applications leading to more demand which in turn leading to more innovations**
- **Interconnect is an important pillar of compute**
  - Compute, storage/ memory, interconnect, software, process technology, security

# EXPLOSION OF DATA ENABLING DATA-CENTRIC REVOLUTION



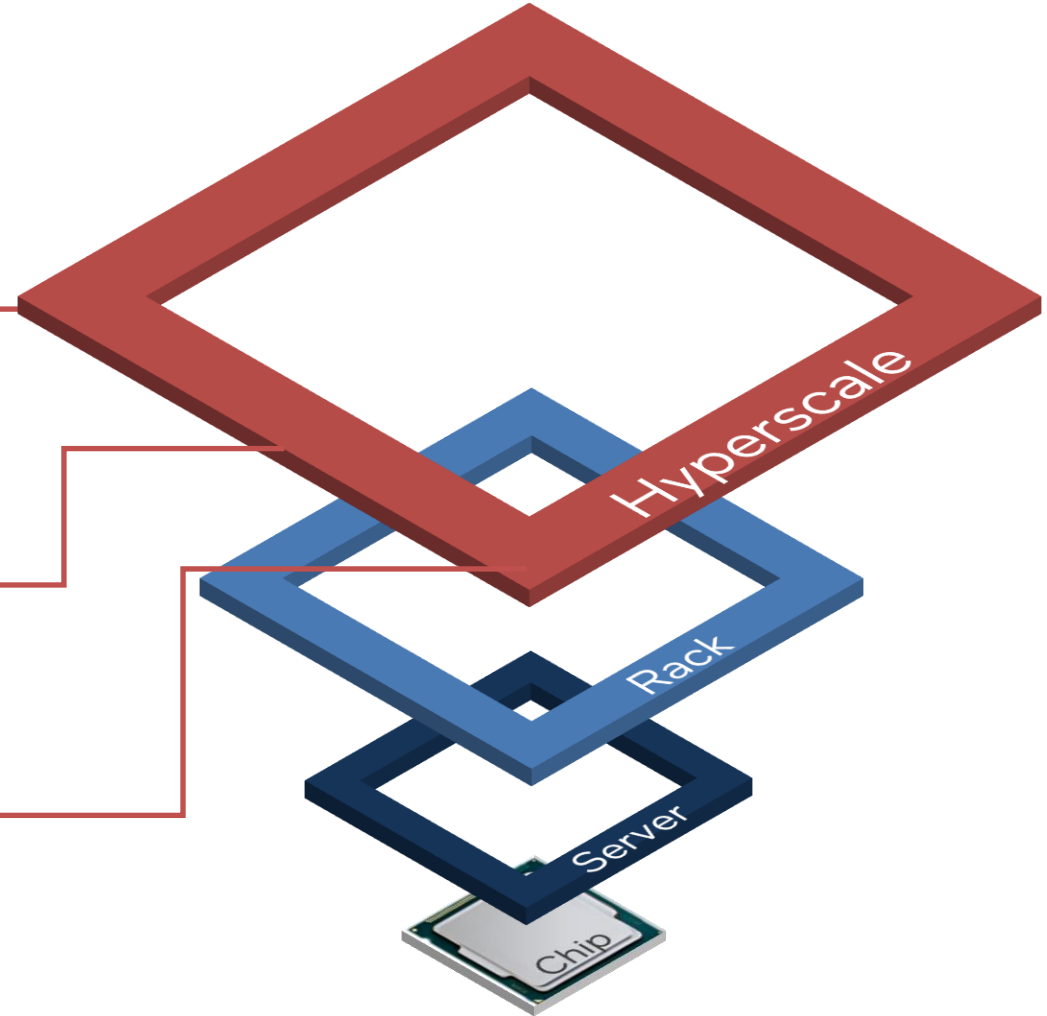
Explosion of data leading to rapid innovations. Move faster, Store more, Process everything seamlessly, efficiently, and securely

# THE VISION

**Seamless**  
Edge to cloud experience

**Predictable and secure**  
services anywhere

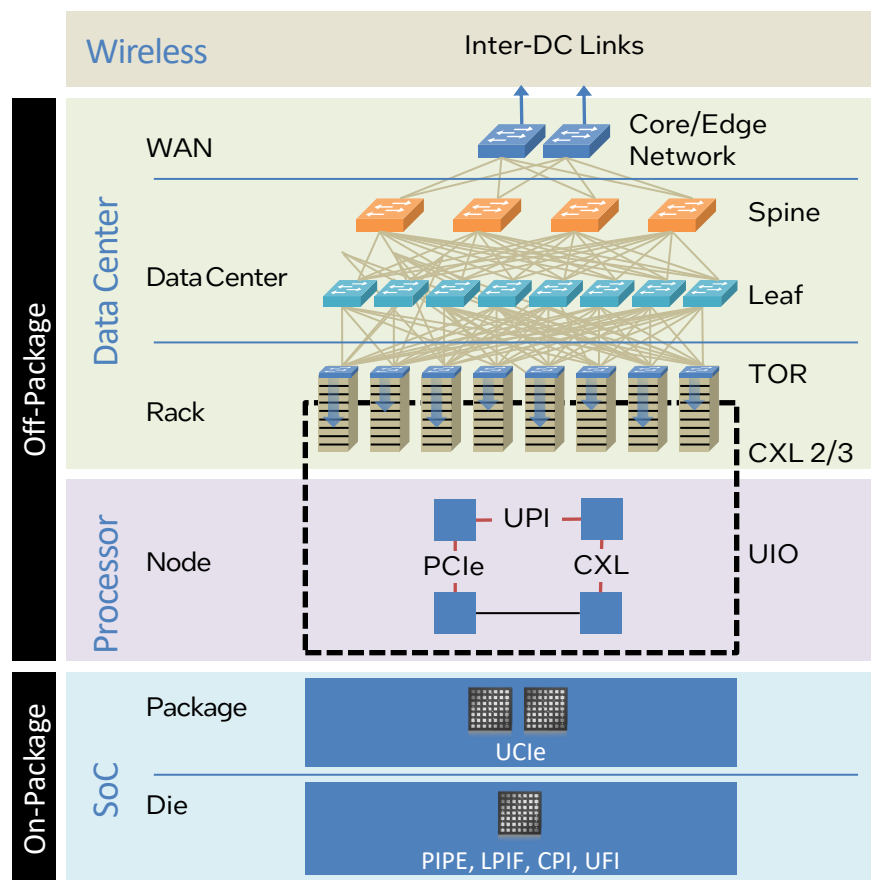
**Optimized TCO**  
Hardware and Software



# AGENDA

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# INTERCONNECTS: TAXONOMY, CHARACTERISTICS AND TRENDS



Source: Intel Corporation

## Networking/Fabric for Data Center Scale

**Latency Tolerant** (Narrow, very high speed)

- 56/ 112 GT/s-> 224 GT/s (PAM4)
- 4-8 lanes, cables/backplane
- PHY latency (Tx + Rx) = 20+ ns (+ >100 FEC)

## Load-Store I/O - Architectural Ordering Semantics

PCIe®/CXL™/SMP Cache Coherency – PCIe PHY) Node (-> Rack)

**Latency Sensitive** (Wide, high speed)

- 32 GT/s (NRZ) -> PCIe Gen6 64 GT/s (PAM4)
- Hundreds of lanes
- Power, cost, Si-area, backwards compatible, latency, on-board -> cables/backplanes
- PHY latency (Tx+ Rx: PHY-PIPE) = <10ns (0-1ns FEC overhead)

## Universal Chiplet Interconnect express (UCle)™ - the new on-package interconnect industry standard

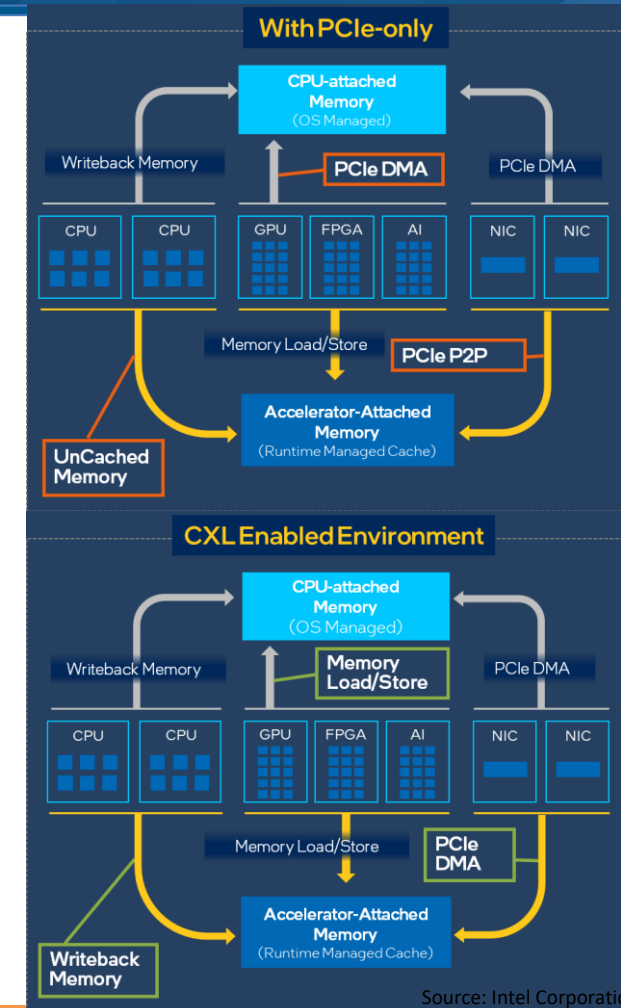
**Latency Sensitive** (Super-wide, high speed)

- 4G – 32G (single-ended, NRZ), 2D, 2.5D (-> 3D)
- Thousands of lanes
- Ultra low power, ultra low latency, high bandwidth density
- PHY latency (PHY – Transaction Layer) = <2ns

Load-Store I/O: from die/ package/node to rack/pod

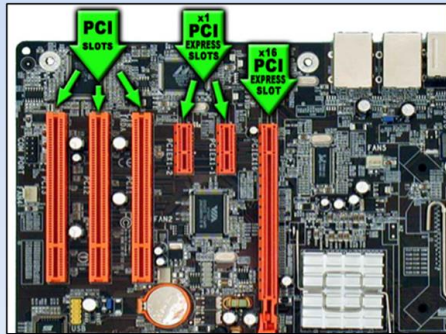
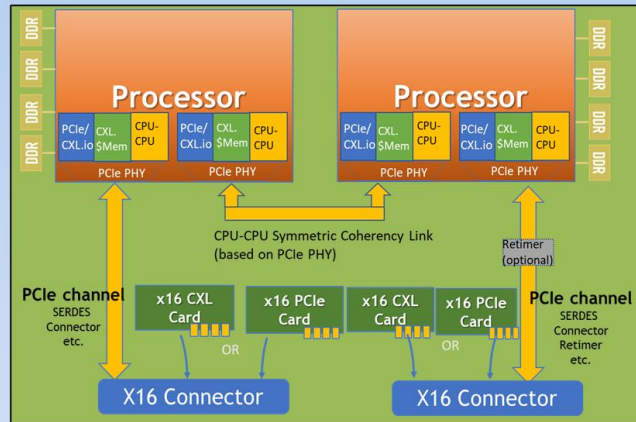
# LOAD-STORE INTERCONNECTS : PCIE AND CXL

- **With PCIe: (900+ member companies)**
  - Memory Connected to CPU – Cacheable
  - Memory Connected to PCIe device is Uncacheable
  - Different Ordering rules across I/O vs coherency domains
  - Ubiquitous I/O for compute continuum
- **With CXL: (~200 member companies)**
  - Caching and memory protocols on top of PCIe
  - Device can cache memory
  - Memory attached to device is cacheable
  - Leverages PCIe infrastructure
- **PCIe and CXL very successful industry standards:**
  - Multi-generational, backward compatible, IP/ tools
  - Compliance program with plug-and-play

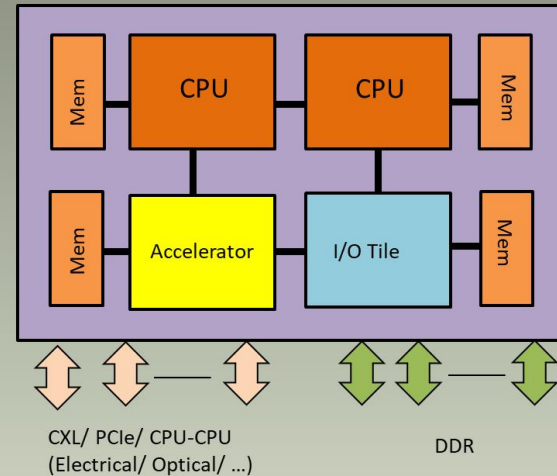
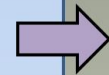


**On-Package Interconnects should leverage PCIe/CXL infrastructure for standardization and Load-Store Usages.. Need to seamlessly move functionality from node to package to die level**

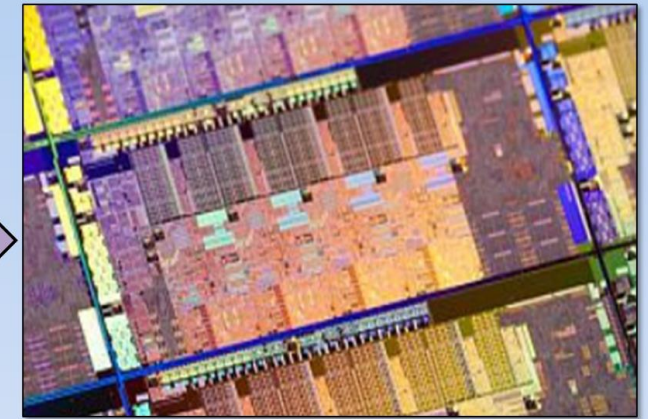
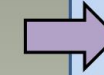
# DESIGN CHOICE: SEAMLESS INTEGRATION FROM NODE → PACKAGE → ON-DIE ENABLES REUSE, BETTER USER EXPERIENCE



Node / Board Level  
Integration



Package Level Integration  
(with on-package interconnects)



On-die Integration

Same Software, IP, and Subsystem to build scalable solutions offers economies of scale , time to market advantage, and seamless user experience. Innovations at the open slot in board level needs to migrate to package level for multiple usages!

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# MOORE PREDICTED “DAY OF RECKONING”



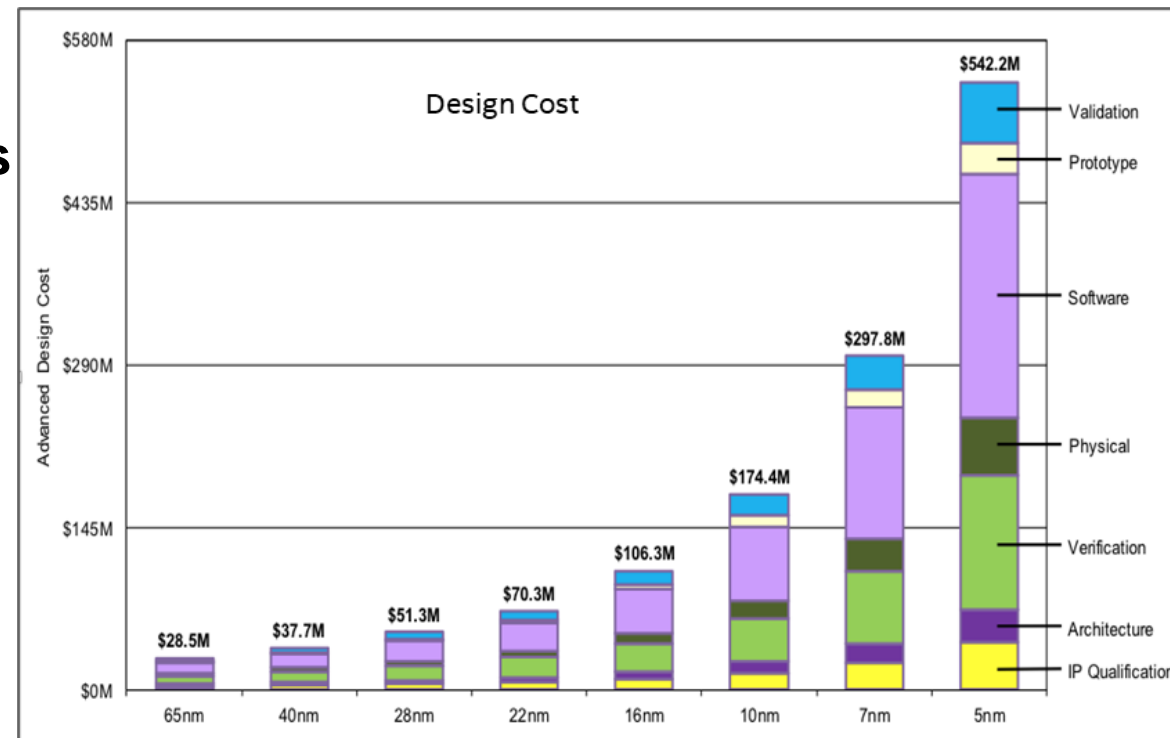
- *“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected<sup>1</sup>.”*

- -Gordon E. Moore

- <sup>1</sup>: “Cramming more components onto integrated circuits”, Electronics, Volume 38, Number 8, April 19, 1965

# DRIVERS FOR ON-PACKAGE CHIPLETS

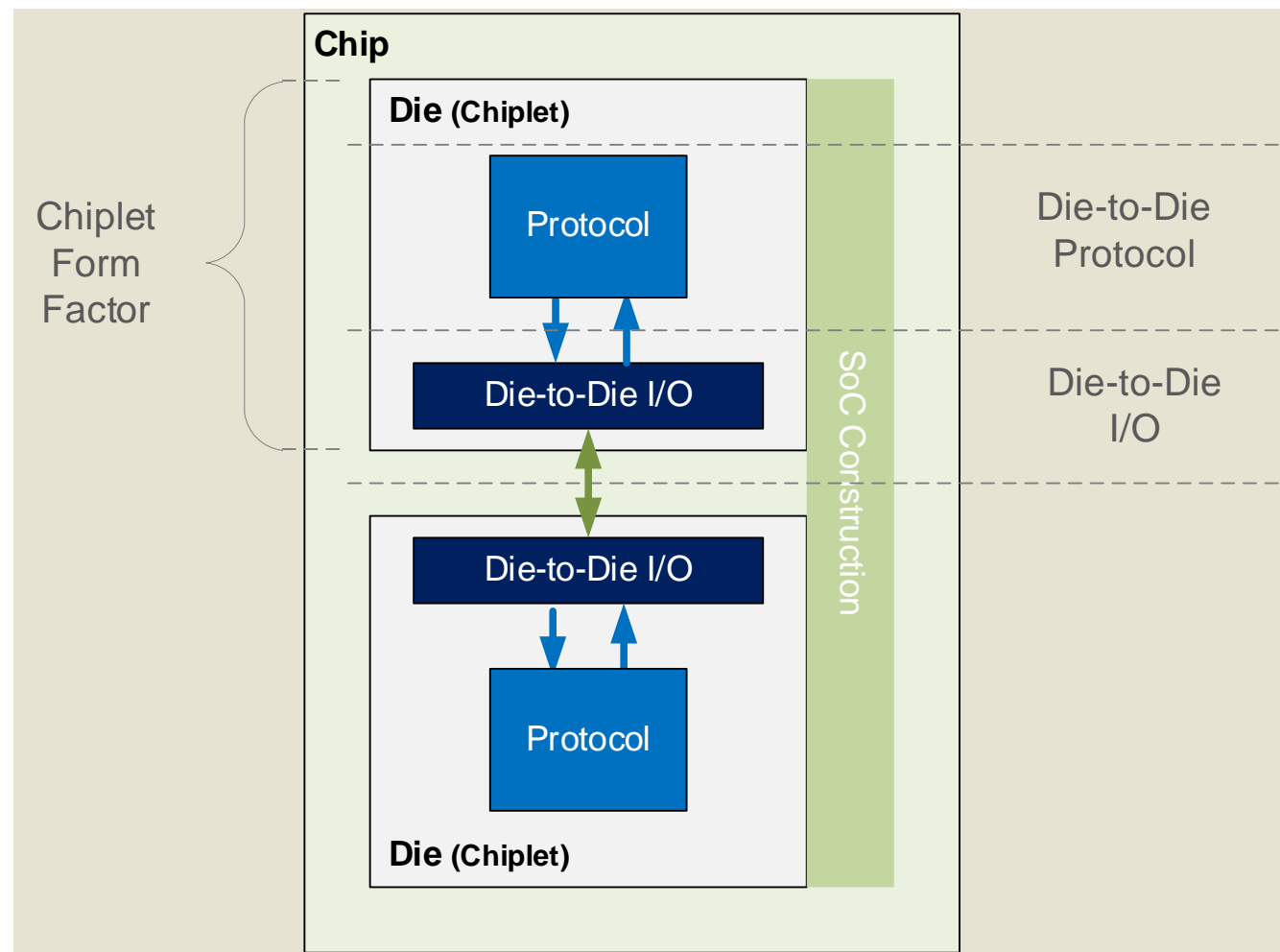
- **Reticle Limit, yield optimization, scalable performance**
  - Same dies on package (Scale-up)
- **Increasing design costs at leading edge process nodes**
  - Die-disaggregated dies across different nodes
  - Use new process node for advanced functionality
- **Time to Market (Late binding)**
- **Custom silicon for different customers leveraging a base product**
  - Different acceleration functions with common compute
- **Different process nodes optimized for different functions**
  - Memory, logic, analog, co-packaged optics
  - High power-efficient bandwidth with low-latency access (e.g., HBM memory)



Source: IBS (as cited in IEEE Heterogeneous Integration Roadmap)

# COMPONENTS OF CHIPILET INTEROPERABILITY

- **Chiplet Form Factor**
  - Die size
  - Bump location
  - Power delivery
  - Thermal characteristics
- **SoC Construction (Application Layer)**
  - SoC Reset
  - Initialization (e.g., fuses)
  - Register access
  - Security
- **Die-to-Die Protocols (Data Link to Transaction Layer)**
  - Link Layer, transaction Layer, etc.: PCIe/ CXL/ Raw/....
  - Internal Interface standardization for plug and play IPs
- **Die-to-Die I/O (Physical Layer)**
  - Bump arrangement and characteristics
  - Electrical & thermal characteristics
  - Substrate or interposer characteristics
  - Length budget, pJ/bit, bit error rate, ...
  - Reset, clocking, initialization, and data transfer
  - Test and repair
  - Technology transition -> multiple bump arrangement/ frequency



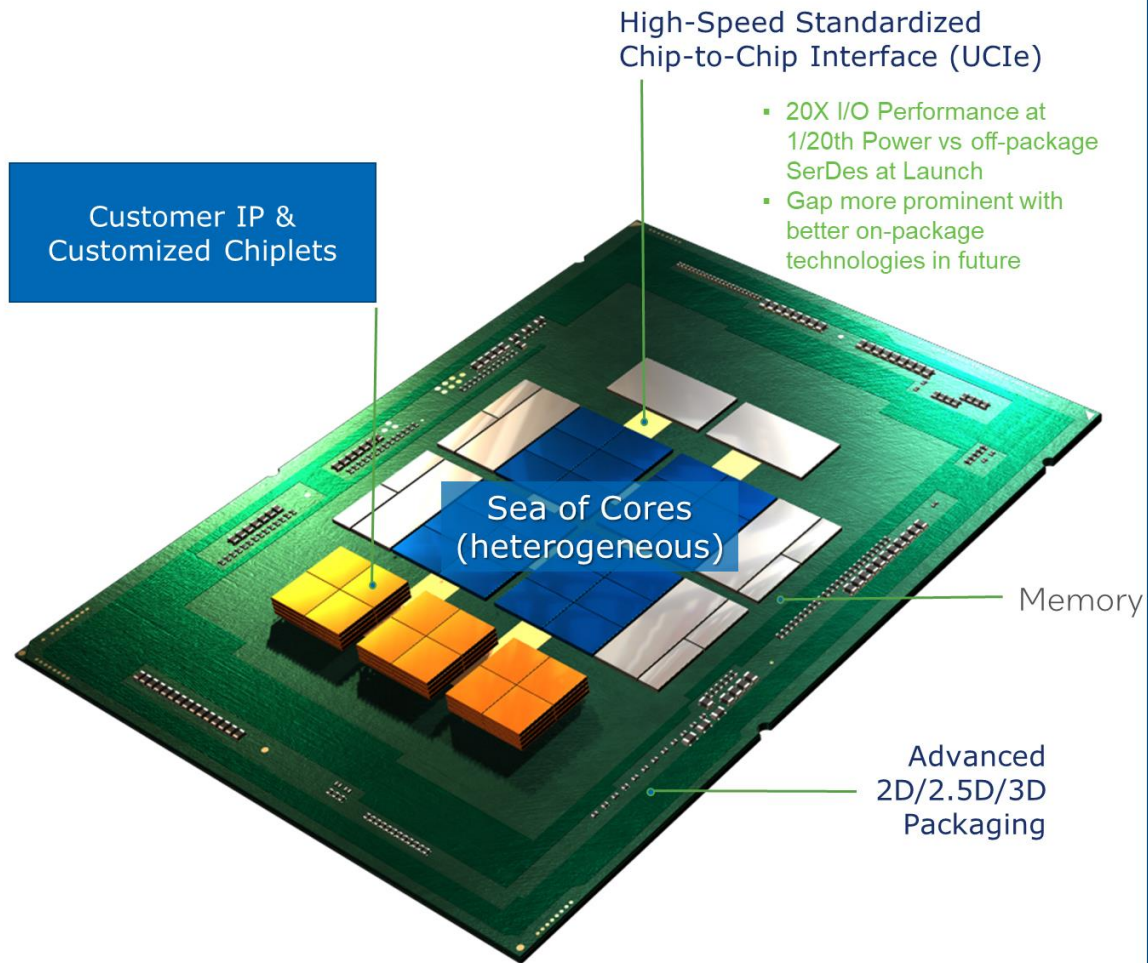
Source: UCIe™ Consortium

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# MOTIVATION FOR UCIE

## OPEN CHIPLET: PLATFORM ON A PACKAGE



- **Enables SoC construction overcoming reticle limits**
  - Package is new System-on-a-Chip (SoC): Scale Up
- **Reduces time-to-solution (e.g., enables die reuse)**
- **Lowers portfolio cost (product & project)**
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- **Enables a customizable, standard-based product for specific use cases (bespoke solutions)**
- **Scales innovation (Mfg process locked IPs)**

UCIe Goal: Align Industry around an open platform to enable chiplet based solutions

# UCIE: KEY METRICS AND ADOPTION CRITERIA

## Key Performance Indicators

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
  - Technology, frequency, & BER
- Reliability & Availability
- Cost: Standard vs advanced packaging

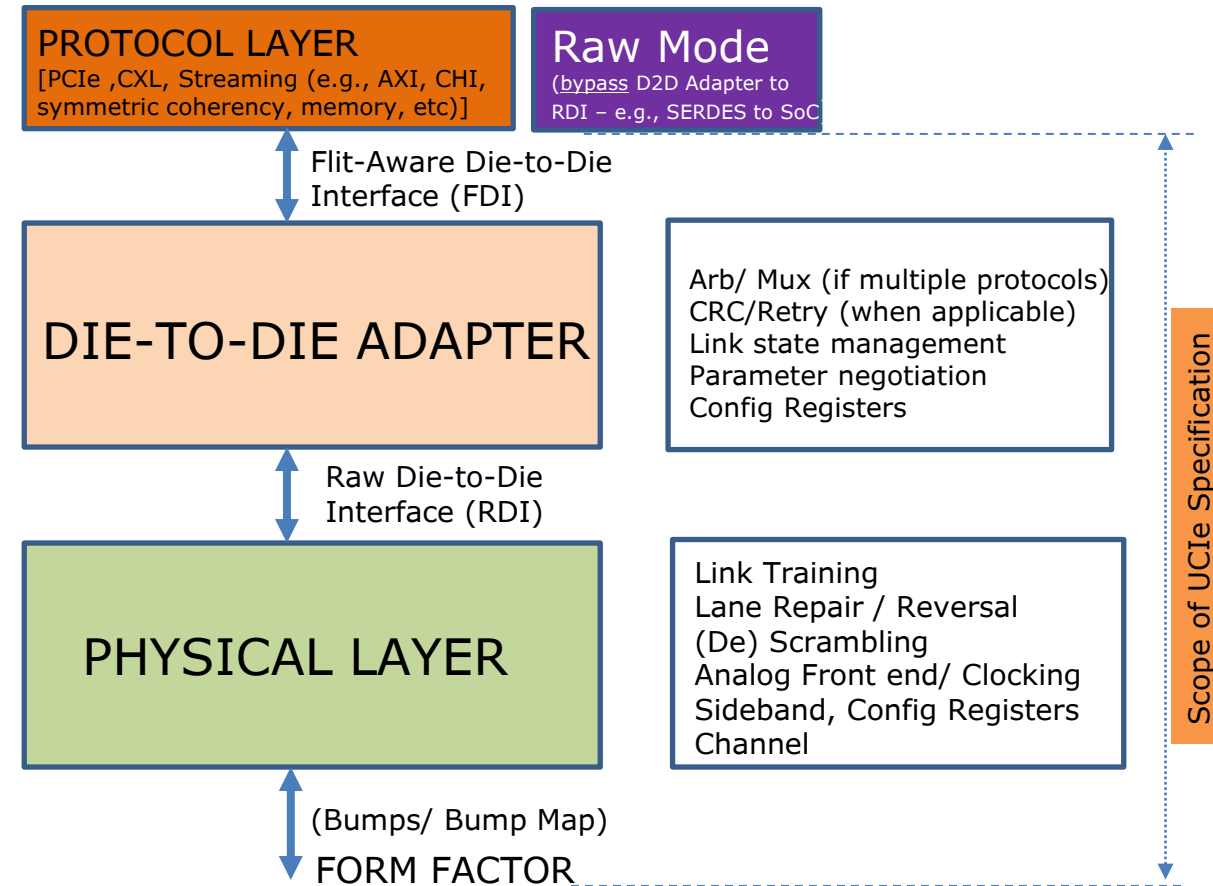
## Factors Affecting Wide Adoption

- Interoperability
  - Full-stack, plug-and-play with existing s/w
  - Different usages/segments - ubiquity
- Technology
  - Across process nodes & packaging options
  - Power delivery & cooling
  - Repair strategy (failure/yield improvement)
  - Debug – controllability & observability
- Broad industry support / Open ecosystem
  - Learnings from other standards efforts

UCIe is architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria

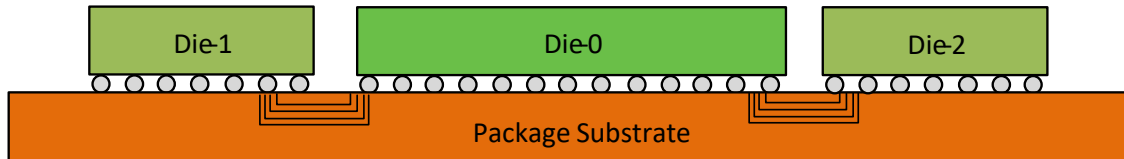
# UCIE 1.0 SPECIFICATION

- **Layered Approach with industry-leading KPIs**
- **Physical Layer: Die-to-Die I/O**
- **Die to Die Adapter: Reliable delivery**
  - Support for multiple protocols: bypassed in raw mode
- **Protocol: CXL/PCIe and Streaming**
  - **CXL™/PCIe® for volume attach and plug-and-play**
    - SoC construction issues are addressed w/ CXL/PCIe
    - CXL/PCIe addresses common use cases: I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
    - Protocol can be anything (e.g., AXI/CHI/SFI/CPI/ etc)
- **Well defined Spec: interoperability and future evolution**
  - Configuration register for discovery and run-time
    - control and status reporting in each layer
    - transparent to existing drivers
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface



Source: UCie™ Consortium

# UCIE 1.0: SUPPORTS STANDARD AND ADVANCED PACKAGES

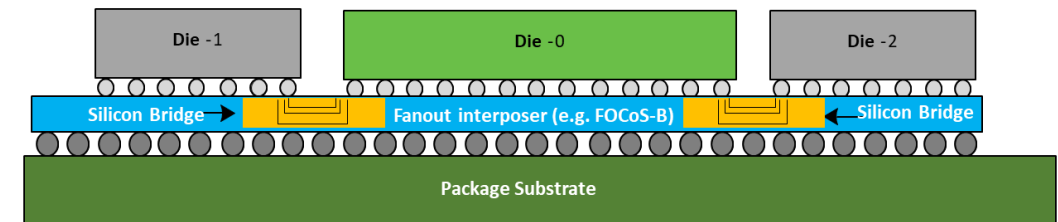
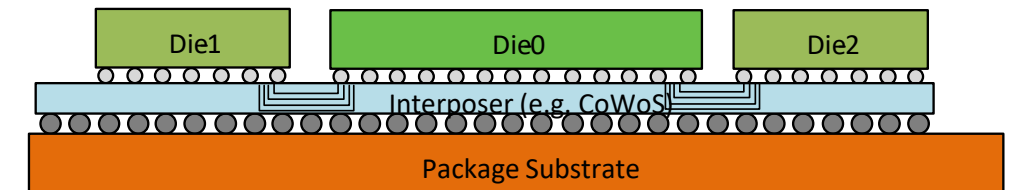
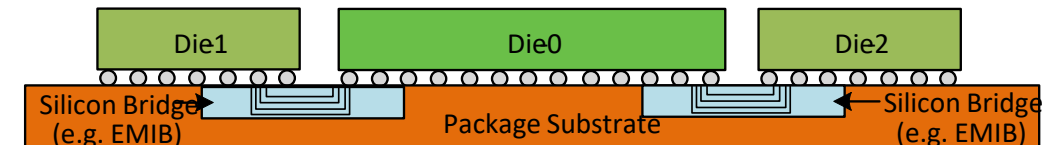


(Standard Package)

Standard Package: 2D – cost effective, longer distance

Advanced Package: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer



(Multiple Advanced Package Options)

Source: UCIE™ Consortium

One UCIE 1.0 Spec covers both type of packaging options

# UCIE PHY: BUMP-OUT FOR INTEROPERABILITY

- **UCIe architected with process portability in mind**
  - Circuit components can be built with common digital/ analog structures
- **Bump-out specified in the specification for interoperability even with future bump-pitch reductions**
  - Die rotation and mirroring supported

txdatasb	txcksb	vccaon	vccaon	rxcksb	rxdatasb
vccio	vss	vccio	vss	vccio	vss
vss	txdata5	txdata7	txckn	txdata9	txdata11
vss	txdata4	txdata6	txckp	txdata8	txdata10
vccio	txdata1	vss	txvld	txdata15	txdata0
vccio	txdata0	txdata3	txtrk	txdata14	txdata1
vss	txdata2	txdata12		txdata13	txdata3

(UCIe-S Unstacked Bump-out)

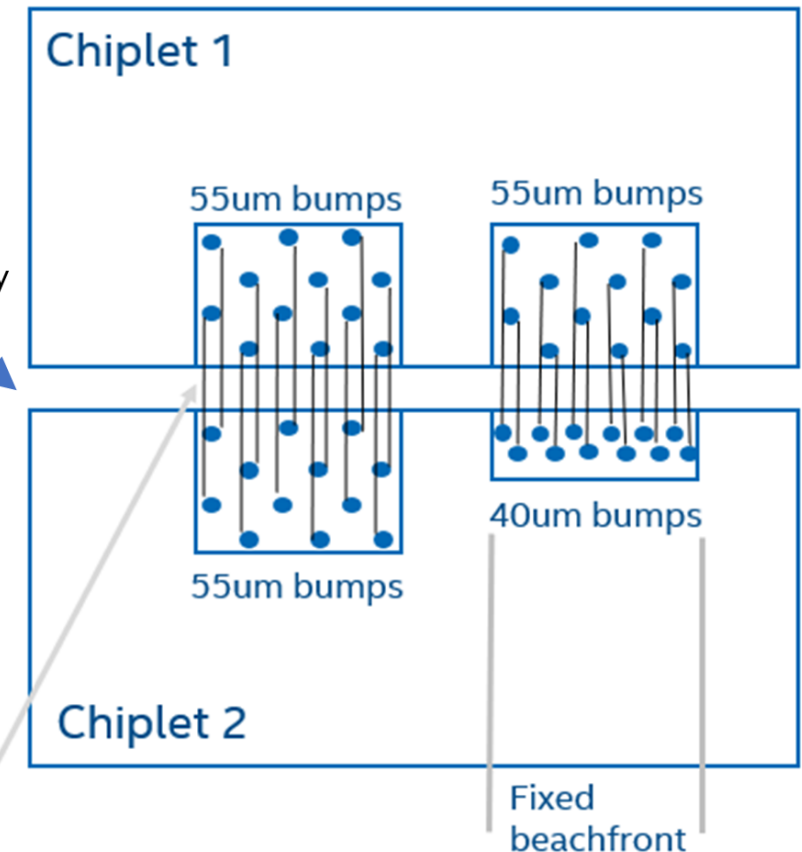
m1txdatasb	m2rxdatasb	m1txcksb	m2rxcksb	vccaon	vccaon	m2txcksb	m1rxcksb	m2txdatasb	vccaon
vss	vccio	vss	vccio	vss	vccio	vss	vccio	vss	vccio
m2rxdata4	m2rxdata6	m2rxckp	m2rxdata8	vss	m2txdata11	m2txckn	m2txdata7	m2txdata5	vss
m2rxdata5	m2rxdata7	m2rxckn	m2rxdata9	vss	m2txdata10	m2txckp	m2txdata6	m2txdata4	vss
m2rxdata0	vss	m2rxtrk	m2rxdata14	vss	m2txdata15	m2txvld	m2txdata3	m2txdata1	vss
m2rxdata1	m2rxdata2	m2rxvld	m2rxdata12	vss	m2txdata13	m2txtrk	m2txdata0	vss	vccio
vccio	vss	vccio	vss	vccio	vccio	vss	vccio	vss	vccio
vss	m1txdata5	m1txckn	m1txdata9	m1txdata11	vss	m1rxdata10	m1rxckp	m1rxdata6	m1rxdata4
vss	m1txdata4	m1txckp	m1txdata8	m1txdata10	vss	m1rxdata11	m1rxckn	m1rxdata7	m1rxdata5
vccio	m1txdata1	m1txvld	m1txdata13	m1txdata15	vccio	m1rxdata14	m1rxtrk	m1rxdata2	m1rxdata0
vccio	m1txdata0	m1txtrk	m1txdata12	m1txdata14	vccio	m1rxdata15	m1rxvld	m1rxdata3	m1rxdata1
vss	m1txdata2	m1txdata12			vss	m1rxdata13			

(UCIe-S Stacked Bump-out)

Fixed beachfront allows for Multi-generational compatibility  
As bump pitches decrease

txdatasb	txcksb	vccaon	vccaon	rxcksb	rxdatasb
vccio	vss	vccio	vss	vccio	vss
vss	txdata5	txdata7	txckn	txdata9	txdata11
vss	txdata4	txdata6	txckp	txdata8	txdata10
vccio	txdata1	vss	txvld	txdata15	txdata0
vccio	txdata0	txdata3	txtrk	txdata14	txdata1
vss	txdata2	txdata12		txdata13	txdata3

(UCIe-A Bump-out)

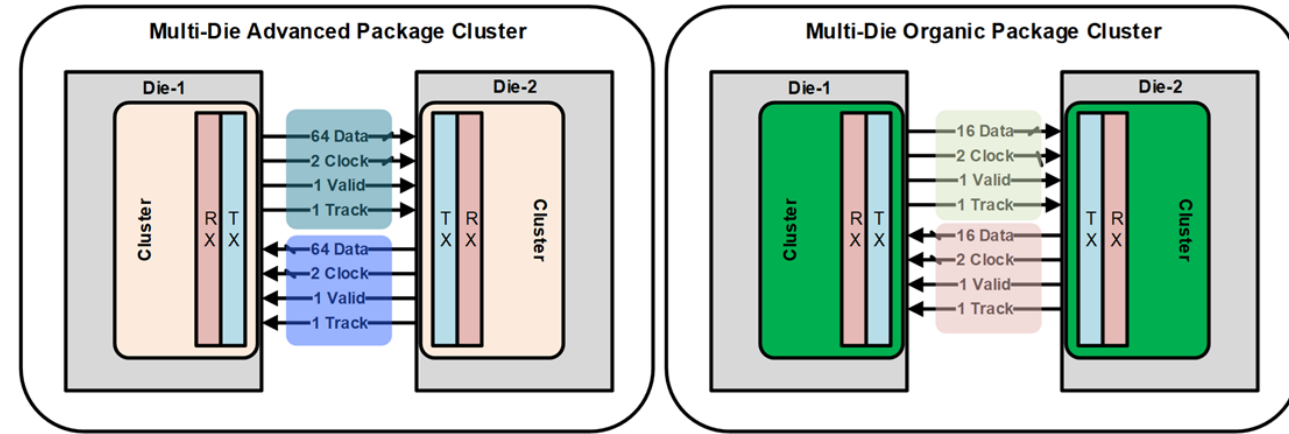


CoWos or EMIB or FoCoS or similar tight-pitch tech

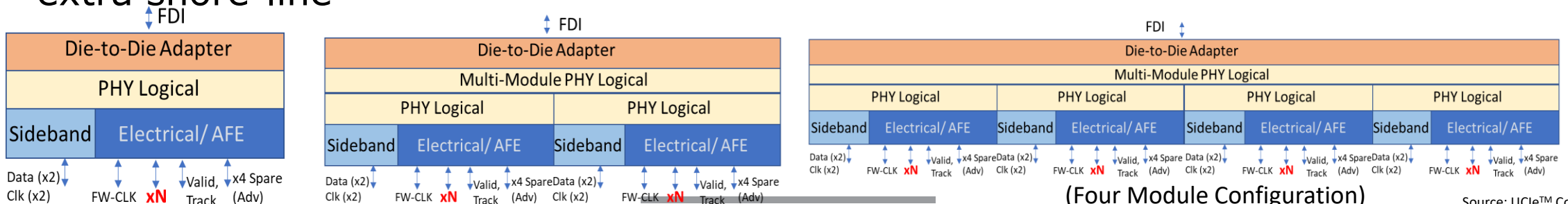
Source: UCIe™ Consortium

# PHYSICAL LAYER

- **Unit is One Module: uni-directional:**  
**1, 2, or 4 modules form a Link**
  - 1 differential pair of forwarded clock
  - Rest are single-ended
  - Data (16/ 64), Valid, Track
  - Valid for effective power management
  - Lane reversal on Transmit side
  - Reliability: Spare Lanes in Adv; degradation in Std
  - Data Rates: 4, 8, 12, 16, 24, 32 GHz
- **Sideband: always on, 800 MHz**
  - 1 data and 1 clock – each direction
  - Used for training, debug, mgmt, etc
  - Depopulated GND bumps to ensure no extra shore-line



Source: UCle™ Consortium



(Single Module Configuration) (Two Module Configuration)

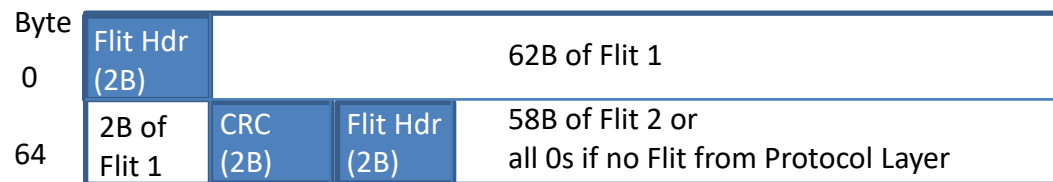
(Four Module Configuration)  
 ( 4-Module Configuration with UCle)

Source: UCle™ Consortium

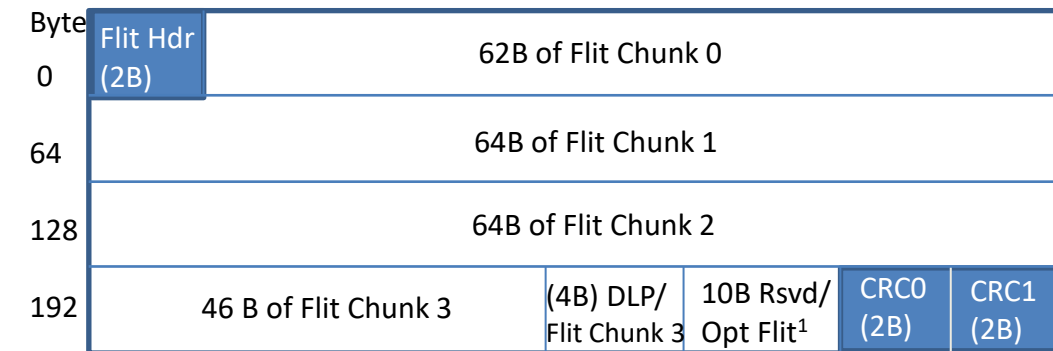
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# D2D ADAPTER AND FLIT MAPPING THROUGH FDI

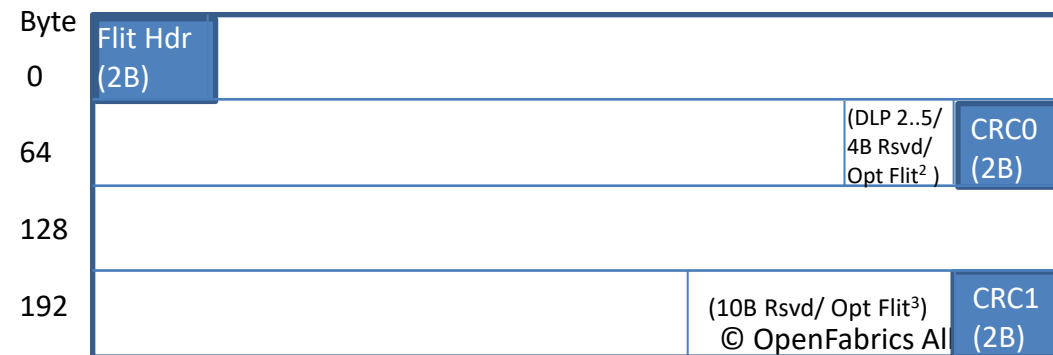
- **Responsible for packetization**
  - Adds Flit Header (2B) and CRC (2B)
- **Supported Flit Sizes: 68B and two flavors of 256B**
  - Decided at negotiation
- **Flit Hdr (2B): Protocol ID (3b), Credit (1b), Flit Ack/Nak management (2b command + 8b sequence number), Rsvd (2b)**
- **CRC: Covers 128B payload (smaller payloads are 0-extended)**
  - Triple bit flip detection guarantee with 16 bits
  - Replay if CRC fails
  - Sample RTL code for CRC provided in the spec



(a. 68-Byte Flit – usage CXL 2.0/ PCIe Non-Flit Mode/ Streaming)



(b. 256-Byte Flit – usage CXL 3.0/ PCIe 6.0)



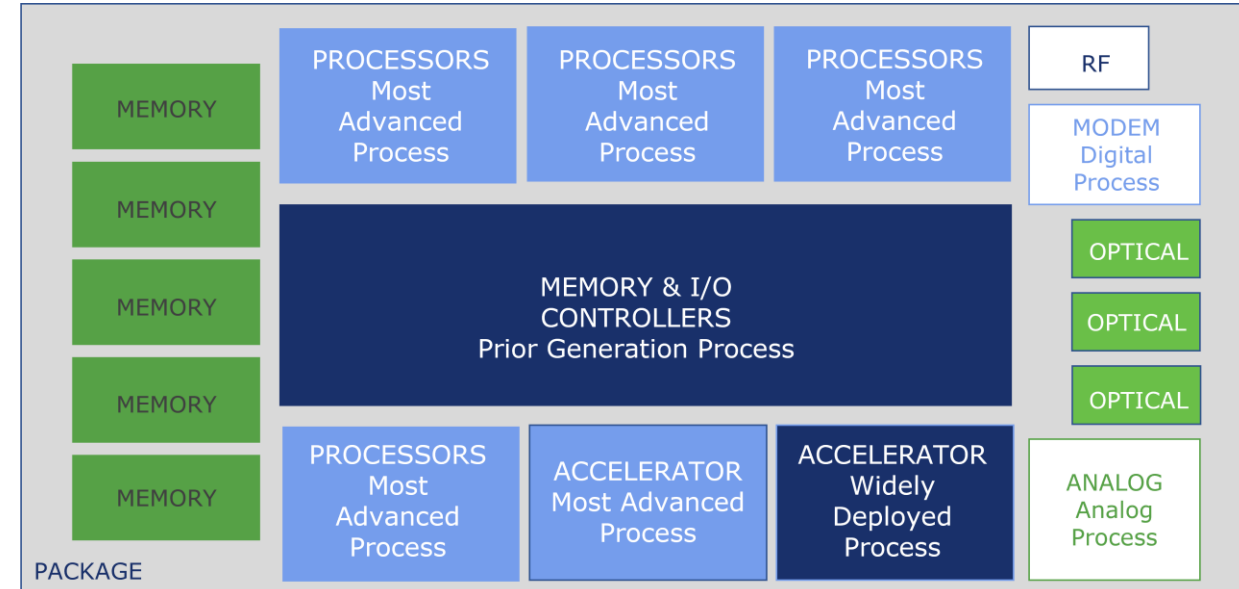
(c. 256-Byte Latency-Optimized Flit – usage CXL 3.0/ Streaming)

Source: UCle™ Consortium

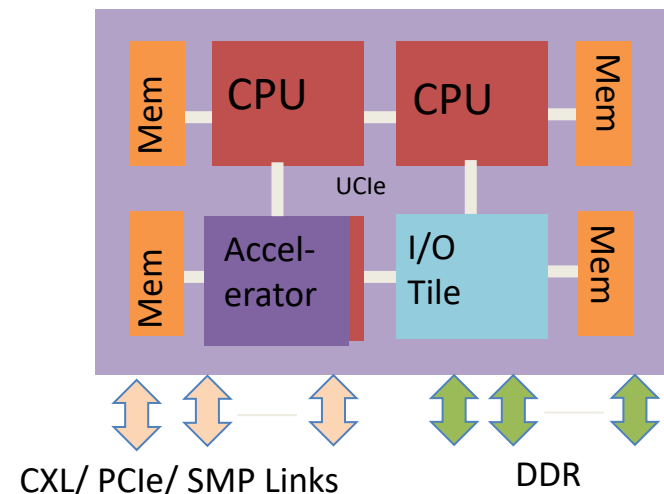
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# UCIE USAGE MODEL: SOC AT PACKAGE LEVEL

- SoC as a Package level construct
  - Standard and/ or Advanced package
  - Homogeneous and/or heterogeneous chiplets
  - Mix and match chiplets from multiple suppliers
- Across segments: Hand-held, Client, Server, Workstation, Comms, HPC, etc
  - Similar to PCIe/ CXL at board level
- Chiplet Types:
  - PCIe/CXL Based: Inference, video, networking (crypto, compression, NIC), memory expansion
  - Streaming: Scale-up, accelerators
  - SERDES: High-speed PHY for PCIe/ Networking (64/ 128G, 112/ 224G)



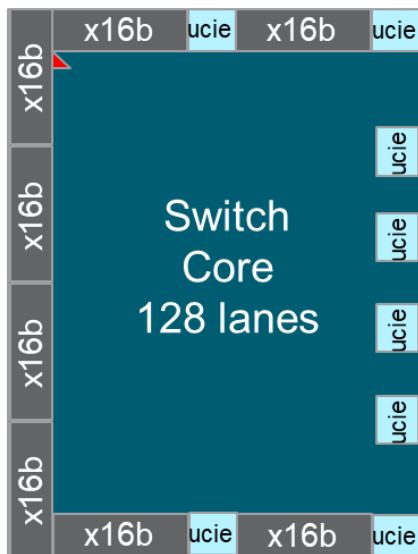
Source: UCle™ Consortium



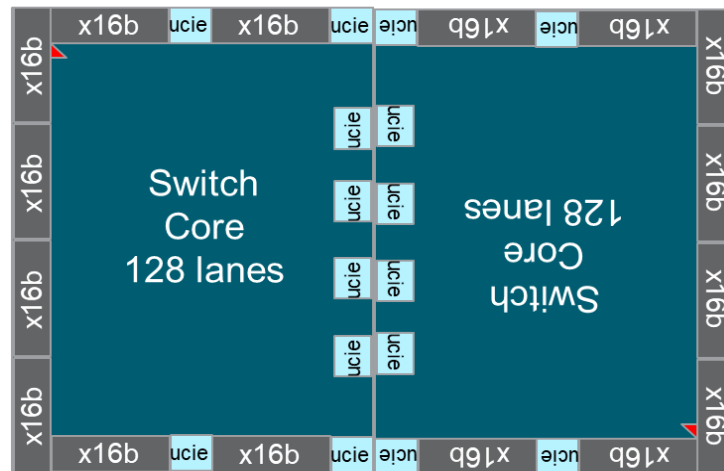
Source: UCle™ Consortium © OpenFabrics Alliance

# EXAMPLE SCALE-UP SOC FROM HOMOGENEOUS DIES: LARGE SWITCH WITH ON-DIE PROTOCOL AS STREAMING OVER UCIE

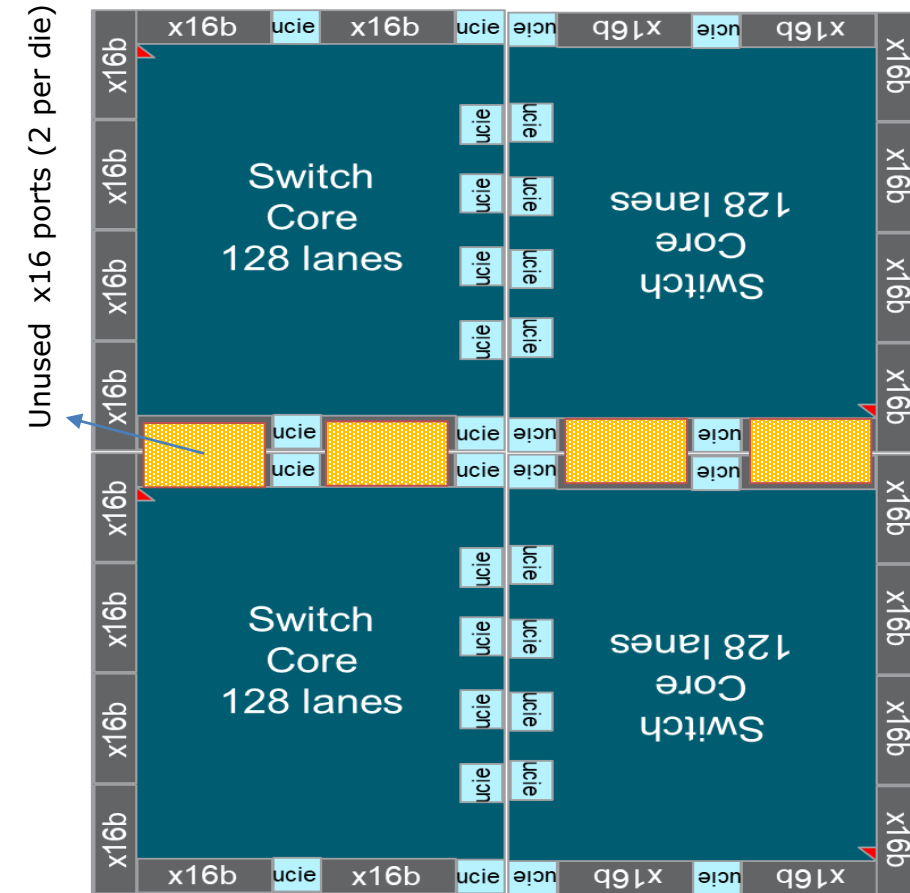
- Need large radix CXL switches
  - challenges: reticle limit, cost, etc.
- UCIE based Chiplets for scale-up
  - 64G Gen6 x16b CXL links
  - UCIE as d2d interconnect – a switch vendor may prefer to have their on-die interconnect protocol be transported over UCIE rather than create a hierarchy of switches which will not work for CXL 2.0 tree-based topology
- Similar approach for other scale-up SoCs (CPU, GP-GPU, N/W Switches)



Small CXL Switch (128 lanes)



Medium-sized CXL Switch (256 lanes)



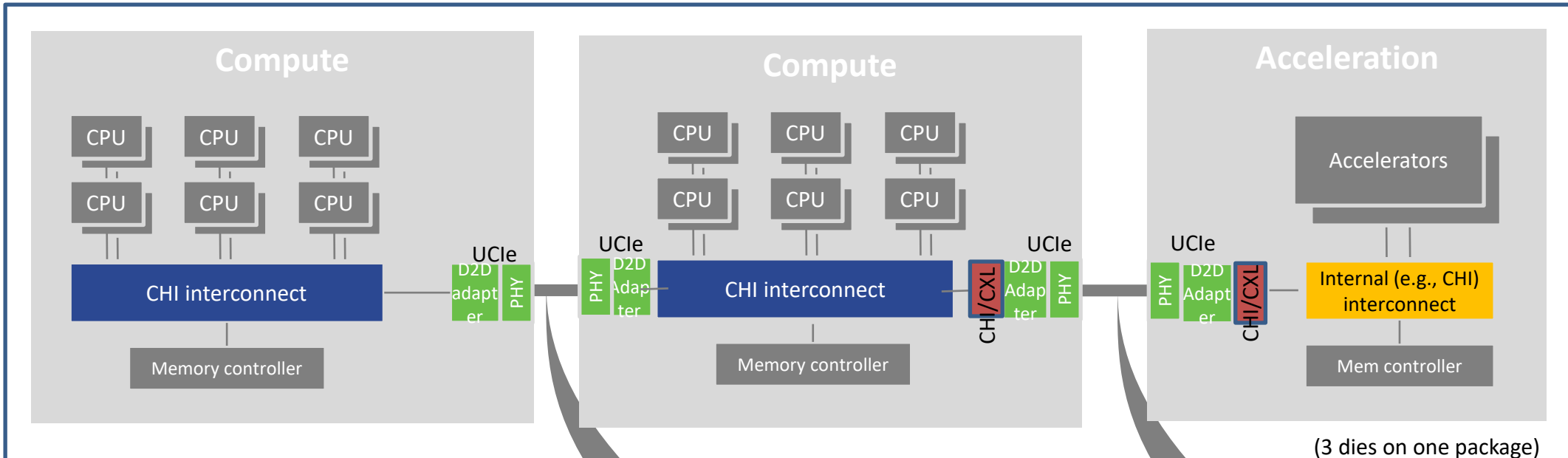
Large CXL switch (512 lanes)

Ack: Nathan Kalyanasundaram

Source: UCIE™ Consortium

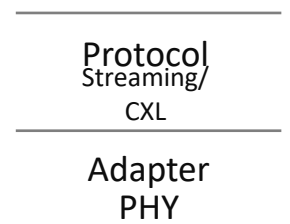
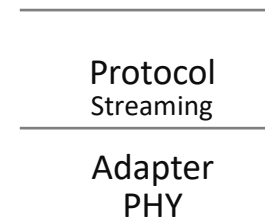
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# EXAMPLE SCALE-UP PACKAGE USING STREAMING AND OPEN-PLUG-IN USING PCIE/ CXL



Not drawn to scale

- Transporting the same on-chip protocol allows seamless use of architecture specific features without protocol conversion
- Streaming interface with additional flit formats provide link robustness using UCIe defined data-link CRC and retry

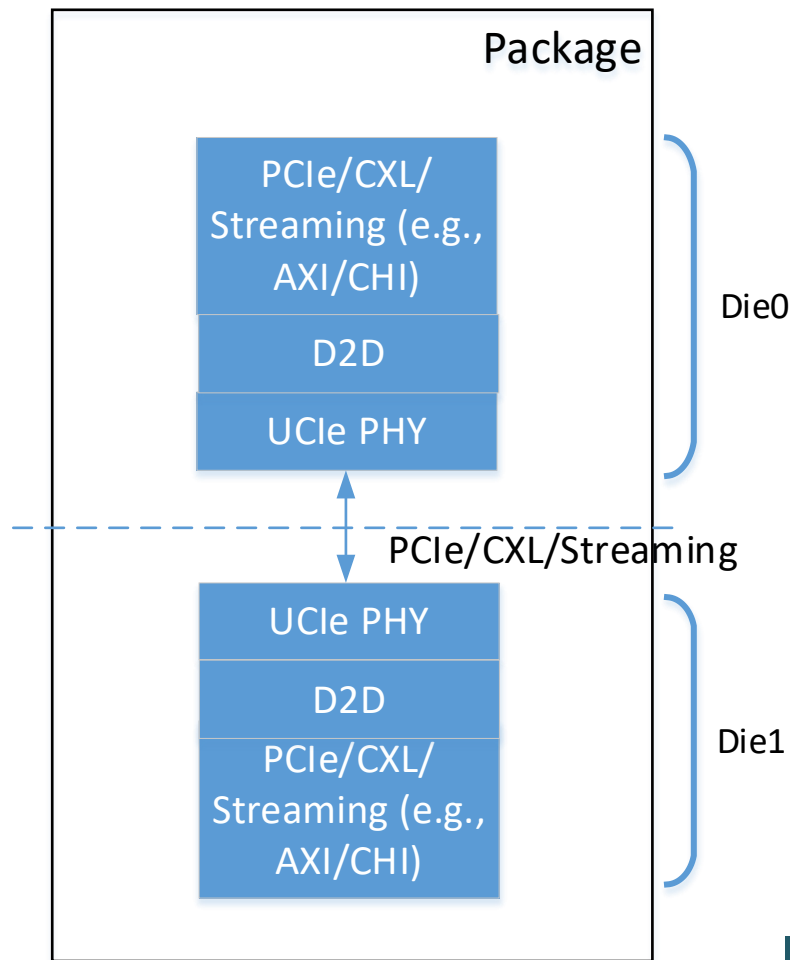


- Any device type in this open plug-in slot with CXL (or CHI if both support it)

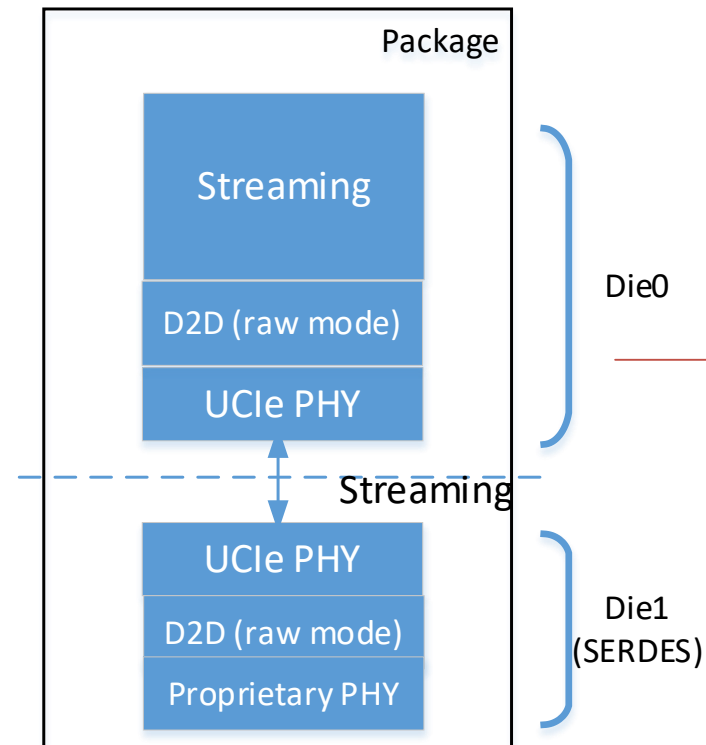
Ack: Marvin Denman, Bruce Mathewson, Francisco Socal, Durgesh Srivastava, Dong Wei

Source: UCIe™ Consortium

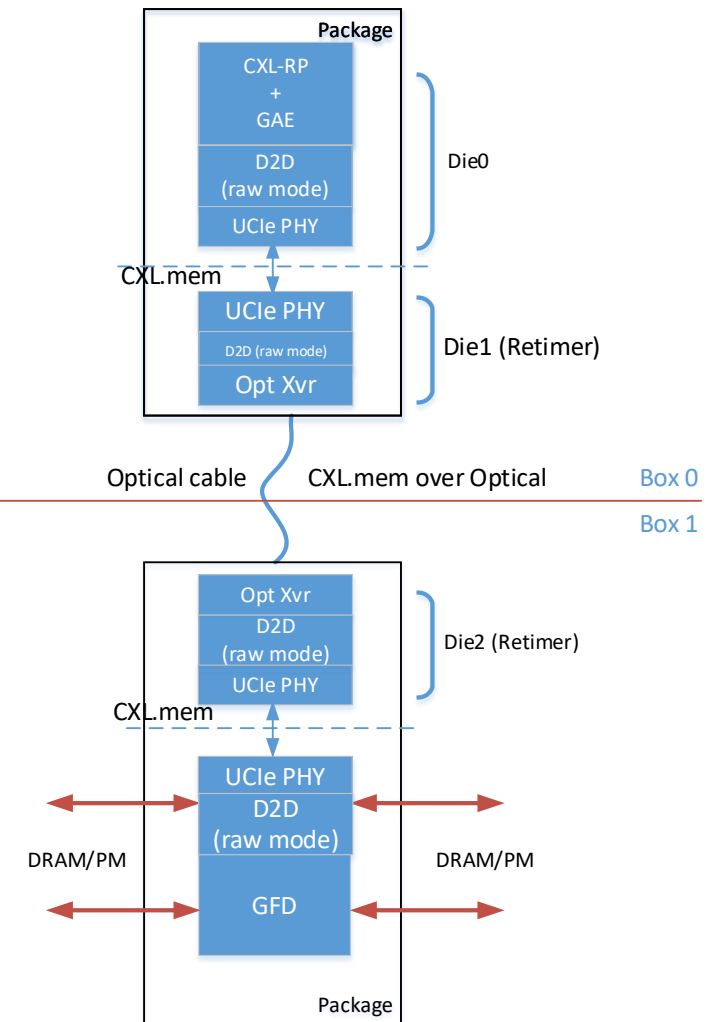
# UCIE BASED SYSTEM TOPOLOGY: SOC AS WELL AS OFF-PACKAGE



Simple PCIe/CXL/Streaming over UCle



Proprietary SERDES solution with UCle



Remote Memory with UCle Optical

# SLIDE FROM MY 2021 OFA KEYNOTE ON FUTURE DIRECTIONS

## ■ Composable Disaggregated Infrastructure at Rack level

- Heterogenous compute/ memory, storage, networking fabric resources
- connected through high bandwidth, low-latency Load-Store Interconnect
- delivering almost-identical performance per watt as independent servers
- w/ multiple domains w/ shared memory, message passing, atomics

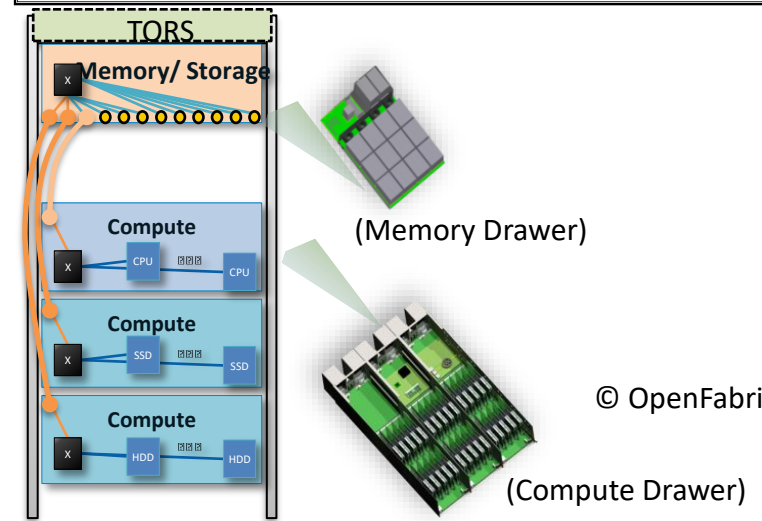
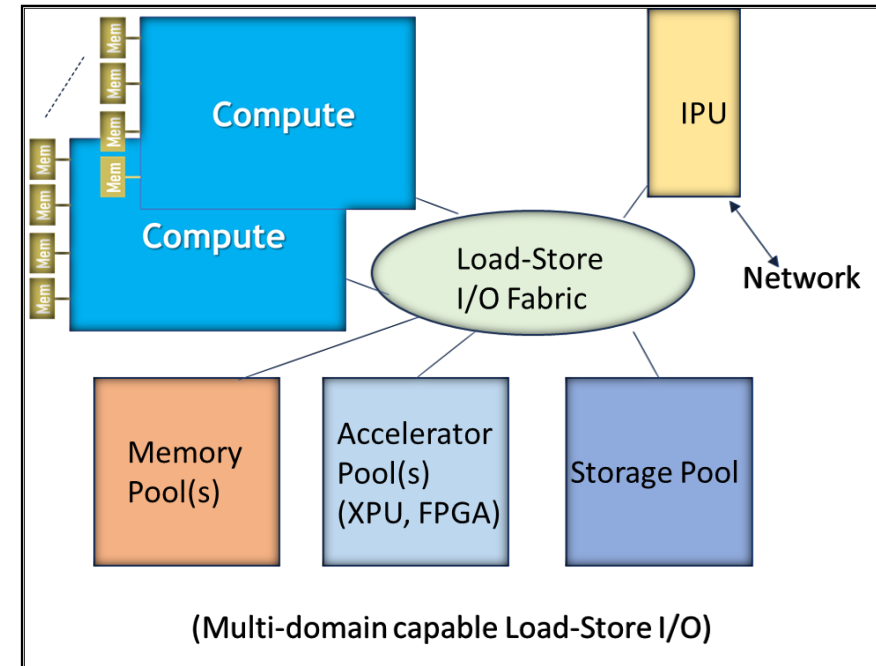
## ■ Synergy between Networking and Load-store

- Expect boundaries to be fungible
- Fabric Manager, Multi-head, multi-domain, Atomics support, Persistence flows, Smart NIC with optimized flows to access system memory without involving host, VM migration

## ■ Challenges:

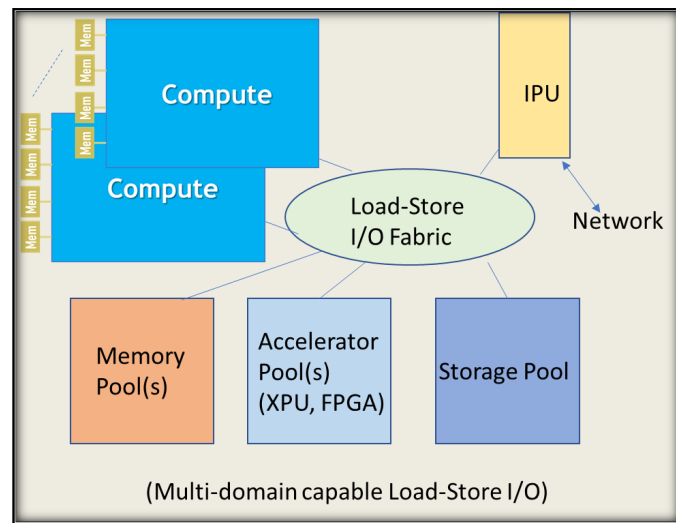
- Latency: NUMA optimization, low-latency switch
- Bandwidth demand: higher rate helps
- Power Efficiency
- Blast Radius – containment and QoS
- Scaling: Moore's law and Dennard-scaling
- Copper-Optical transition point
- Software!

Key Takeaway (2023): CXL Protocol for Rack/Pod level dis-aggregation/ scale-up  
UCle PHY for on-package and co-packged optics for Rack/Pod  
PCIe/ CXL PHY for board/ Rack level



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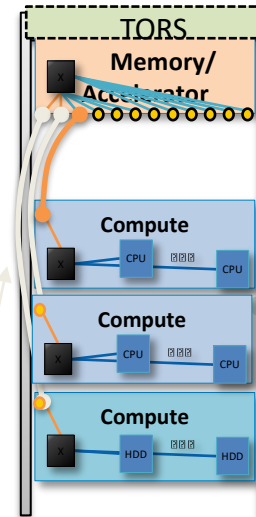
# UCIE USAGE: OFF-PACKAGE CONNECTIVITY WITH UCIE RETIMERS



(Vision: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/ sharing as well as message passing)



(Pod of Racks)

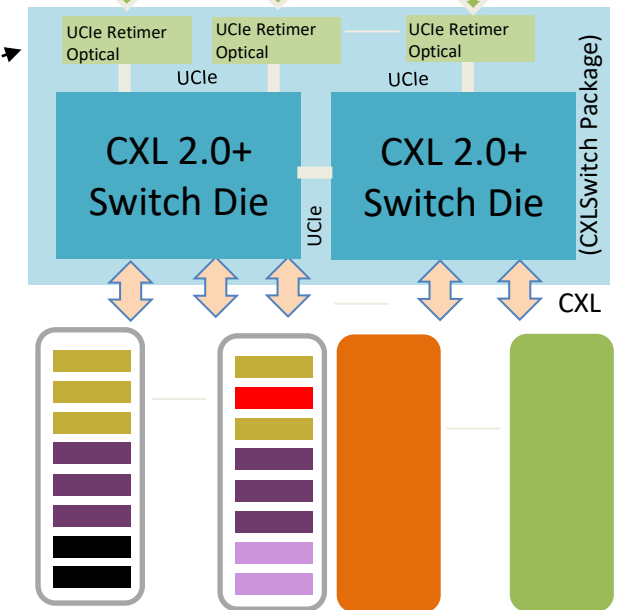


(Compute Drawer)

CXL Rack / Pod level connected using long-reach media (Electrical/ Optical/ ..) through UCle Retimers (e.g., co-packaged optics)

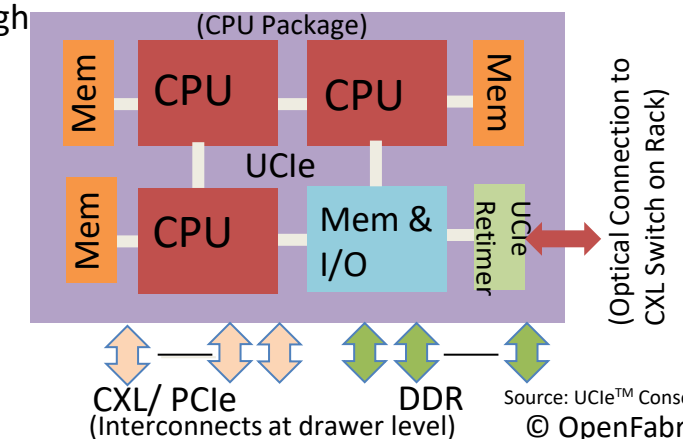
(Physical Connectivity using UCle-Retimer based co-packaged optics)

(Optical connections: Intra-Rack and Pod)



(Pooled/ Shared Memory)

(Pooled Accelerator)



Rack/ Pod Level resource pooling/ sharing with UCle

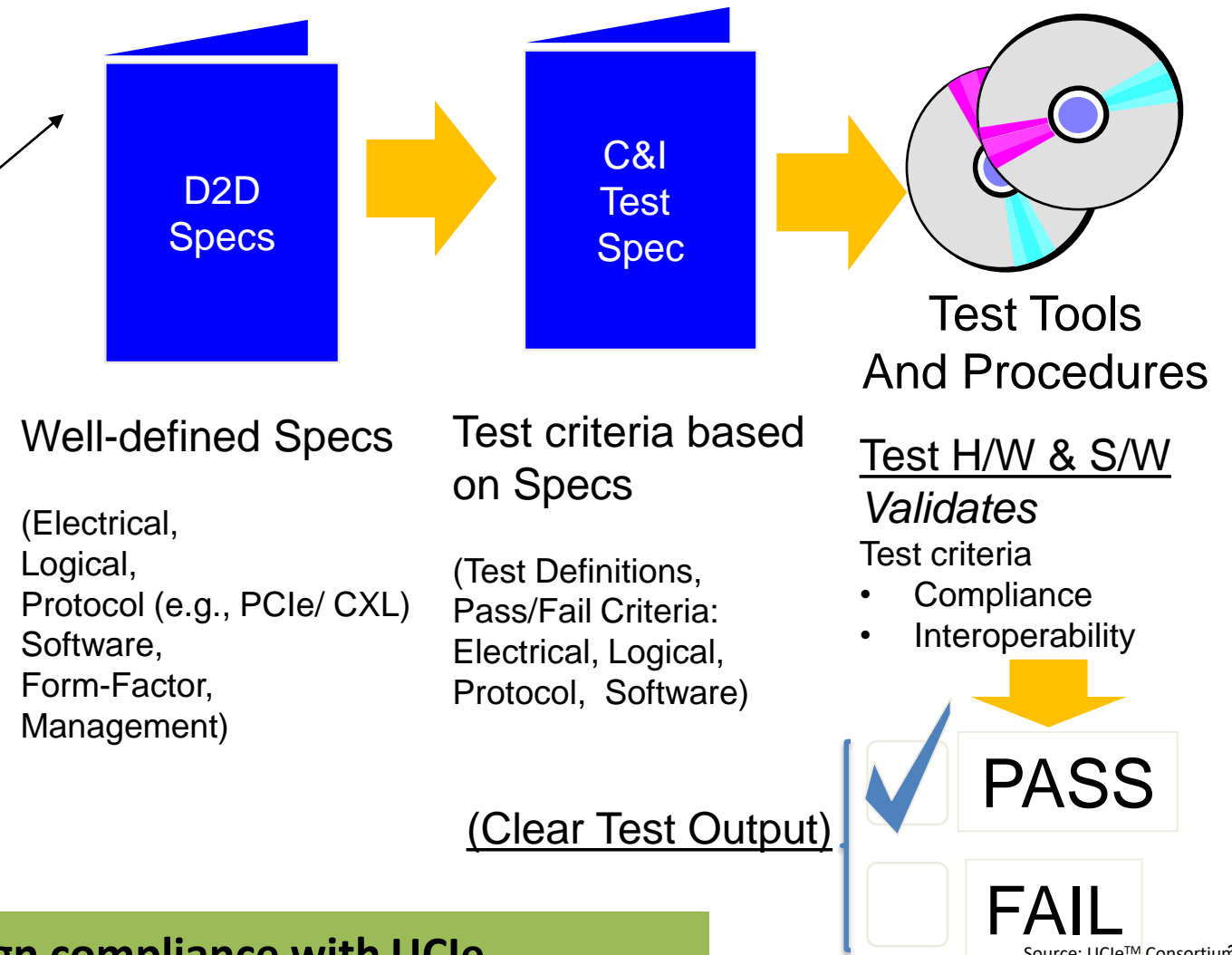
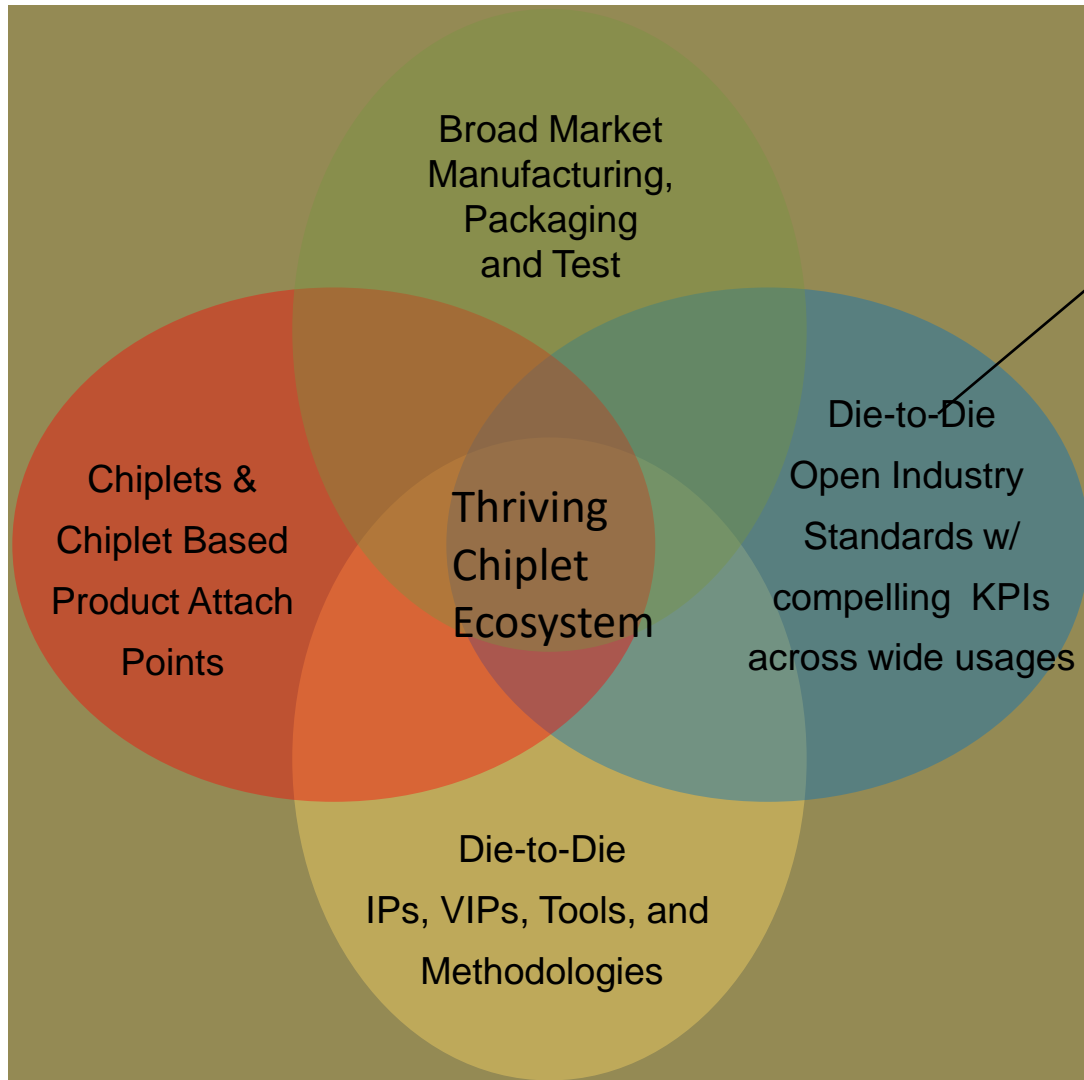
# UCIE 1.0: CHARACTERISTICS AND KEY METRICS

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm <sup>2</sup> )	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIE Flit Mode

UCIE 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years.  
Wide industry leader adoption spanning semiconductor, manufacturing, assembly, & cloud segments.

# INGREDIENTS OF BROAD INTER-OPERABLE CHIPLET ECOSYSTEM



**Predictable path to design compliance with UCle**

# 100+ Member Companies Board Members

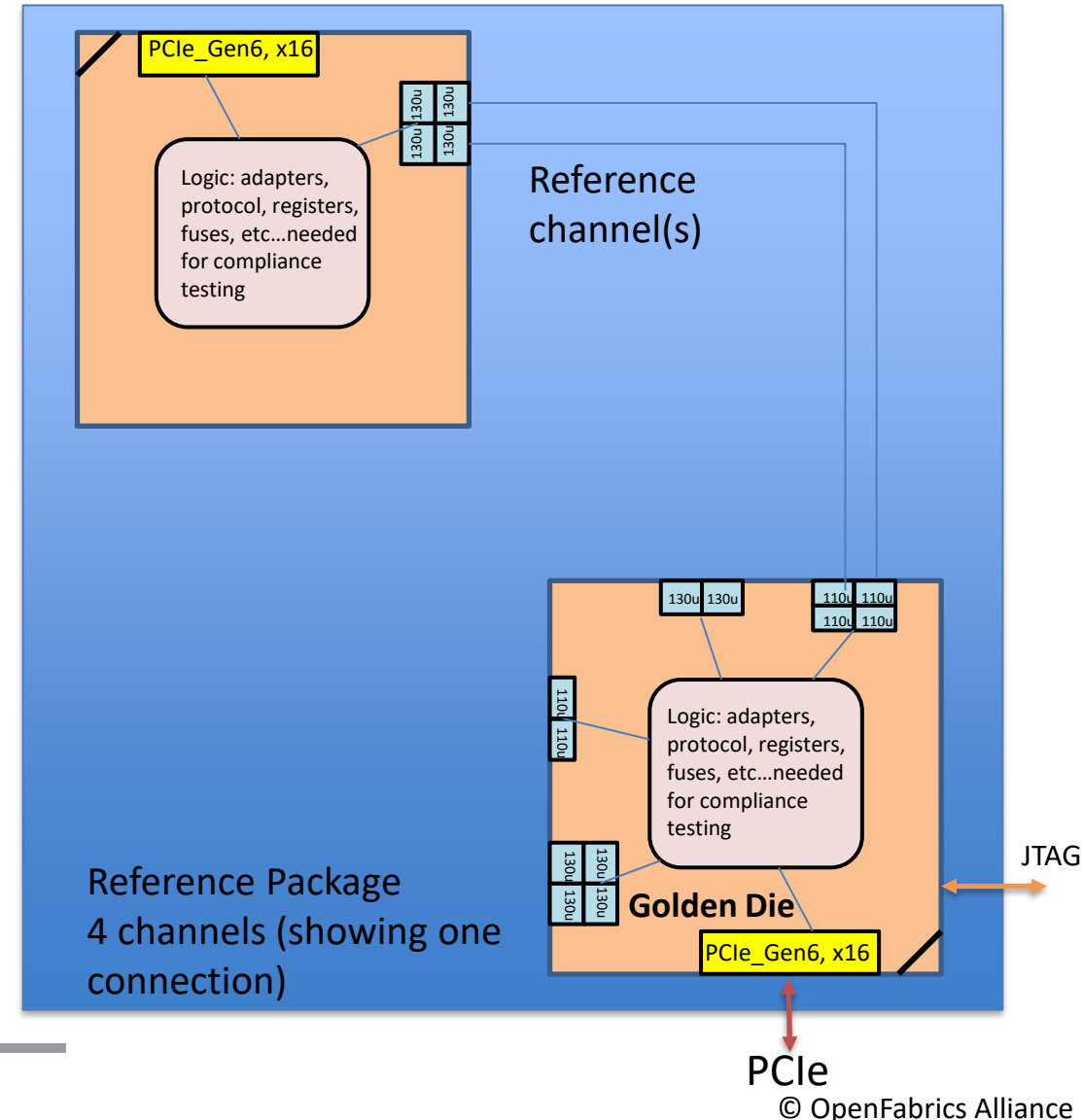


Leaders in semiconductors,  
packaging, IP suppliers,  
foundries, and cloud service  
providers are driving  
the open chiplet ecosystem.

**JOIN US!**

# FUTURE DIRECTIONS: COMPLIANCE TESTING

- **Golden Die is self tested with another golden die**
  - calibrate the channels on the reference package
- **UCle Devices tested against golden die for the following:**
  - Physical layer: training, channel spec compliance, eye height/ width, BER, Tx swing, Rx voltage
  - Adapter layer: CRC, error detection/ replay, etc.
  - Protocol layer: PCIe and CXL – leverage the respective protocol compliance suite
  - Assumption: DUT passes the sort and HVM prior to compliance
- **Sideband plays a critical role to gather information on training and subsequent progression**
- **Formal compliance program needed (similar to PCI-SIG, CXL, USB)**



# FUTURE DIRECTIONS

## ■ Challenges to solve:

- Set of foot-prints for chiplets
- Power delivery, Cooling
- Debug and test
  - Not all chiplets are accessible and UCle can not be probed on a package
  - Need a mechanism for controllability and observability from external package pins

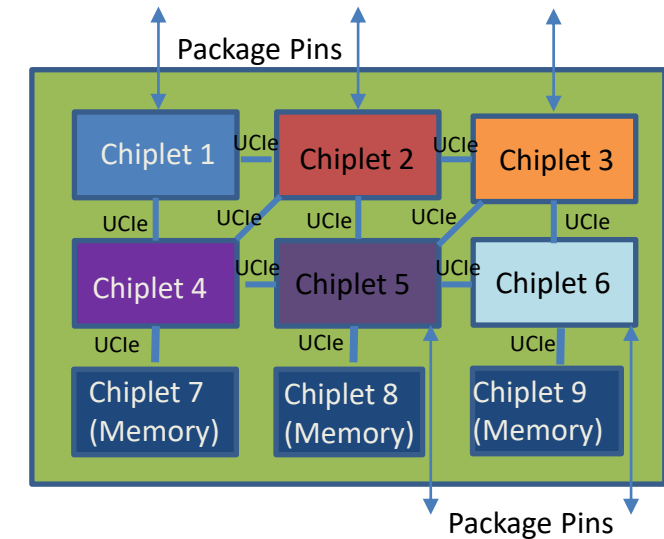
## ■ Protocol Enhancements: Native on-package memory

## ■ Reduced bump pitches with advanced packaging:

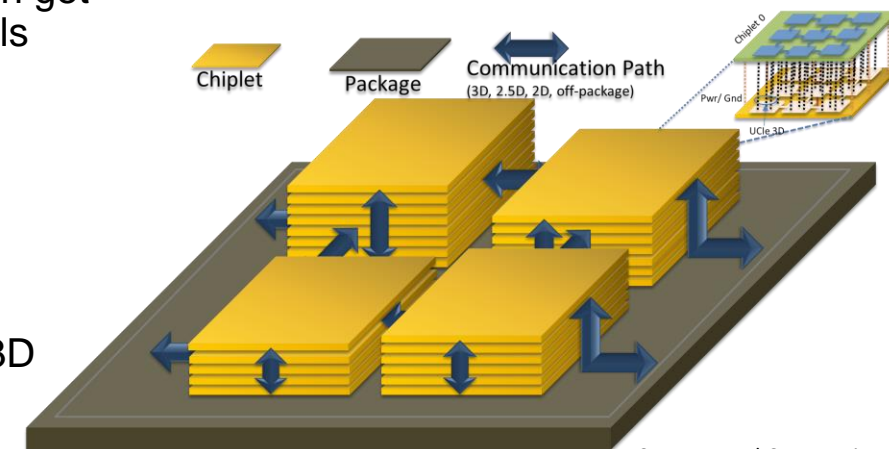
- B/W density will increase as a square of the pitch reduction (e.g., pitch goes down from 45u -> 25u => B/W density will go up by 3.24X)
- Higher B/W => Reduced frequency (say 1/2) so that we still get higher b/w but can get power savings with simpler circuit (reduces capacitance) and lower voltage levels ( $CV^2f$ ) – get benefit of C and V reduction

## ■ 3D chiplets

- 3D power-efficiency and latency will approach on-die levels
- Challenges: Reliability, debug, power delivery, cooling
- Combination of 3D, 2.5D, and 2D integration on package
- Interconnect b/w and power will be a challenge – skyway interconnects across 3D towers on package?



Source: Intel Corporation



Source: Intel Corporation

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# CONCLUSIONS

- **Chiplets and D2D interface are essential to the compute continuum**
  - **Power-efficient performance, yield optimization, different functions, custom solutions, cost-effective**
- **UCle standardization will propel the development an open ecosystem**
  - **Open plug-and-play “slot” at package level will unleash innovations**
  - **Evolution needs to track the underlying packaging technology to deliver compelling metrics**
  - **Form-factor, New Protocols, and manageability are some other areas for innovation**
- **The open chiplet journey with UCle just started! Join us in what will be an exciting journey for decades!**



2023 OFA Virtual Workshop

**THANK YOU**

**Dr. Debendra Das Sharma**

**Chair, UCle Consortium**

**Intel Senior Fellow and co-GM Memory and I/O Technologies, Intel Corporation**