ML model size and GPU performance over the past 10 years

- ML model size over 10 years: ~8600x
  - Exponential growth from 61M in 2012 to 530B in 2021
- AMD GPU performance over 10 years: ~50x
- ML model size has outpaced the growth in single GPU performance over the past 10 years
Ethernet speeds over the past 40 years

- ML model size over 10 years: ~8600x
- AMD GPU performance over 10 years: ~50x

- Ethernet speed over 10 years: ~10x
  - Significantly slower than GPU advancement and ML model size growth

- Emergence of scale-out architectures
  - A sea of heterogeneous nodes connected via the high-speed network

*Source from Ethernet Roadmap 2023 by Ethernet Alliance*
Emergence of scale-out architectures

- A sea of nodes connected via high-speed and low-latency network interconnect

- Heterogeneity within a node
  - CPUs, FPGAs, GPUs, ASICs (such as TPs), SmartNICs …

- SmartNIC acts as an intermediate hub for various components
  - Regular “NIC” functions: protocol handling, vSwitch, crypto, …
  - Value-add “NIC” functions: TOE, RDMA, security, telemetry, …
  - Upper layer processing: transport-layer and above, accelerate streaming and lookaside applications

- High-speed and low-latency networking: RDMA
Data communication in scale-out setups

- Traditional way incurs multiple data copies
- Programmable SmartNIC-enabled system – zero copy

1. Enable direct memory access among peers
2. Bring data as close to compute as possible
What kind of programmable SmartNIC features do we need in a scale-out system?

- Normal network packets
  - TCP, UDP, DCCP, SCTP, QUIC, …
- Remote direct memory access (RDMA)
  - RoCEv2 packets
  - Shared by host, GPU and FPGA
- Bring data as close to accelerators as possible for fast and adaptable hardware acceleration
  - Compute logic for general applications inside SmartNIC
    - Streaming computation
    - Lookaside computation
Why RecoNIC?

- RDMA is the de facto standard for high-speed data communication for ML & HPC applications
- Basic Adaptive SmartNICs without transport-layer offloading engine
  - OpenNIC [1]
  - Corundum [2]

Stand-alone transport-layer offloading engines
- Catapult LTL engine [3]
- TCP offloading engine [4] and RDMA [5] from ETH Zurich
- ERNIC [6]
  - An RDMA engine from AMD
  - RoCEv2 implementation

There is no open-sourced RDMA-enabled adaptive SmartNIC platform
RecoNIC: RDMA-enabled Compute Offloading on SmartNIC

- An open-source 100Gb/s FPGA-based SmartNIC infrastructure/testbed with RDMA and compute offloading
- To enable scale-out heterogeneous systems
- To enable direct memory access among network-connected peers
- To bring data as close to various types of accelerators as possible
The RecoNIC system architecture

- A hardware shell
  - RDMA engine: shared by host and accelerators
  - Compute boxes for streaming and lookaside acceleration
  - Packet classification
  - Auxiliary components
    - MAC, QDMA, crossbars, arbiter

- Software stacks
  - Network stacks
    - non-RDMA traffic such as TCP/IP, UDP/IP and ARP
    - User-space RDMA APIs
  - Memory driver
    - data transfers between host and device memory
  - Control driver
    - Register configuration control
    - Compute control
The RecoNIC network flow

- Non-RDMA traffic
  - **TX path**: Network stack -> QDMA subsystem TX -> Arbiter -> MAC subsystem TX
  - **RX path**: MAC subsystem RX -> Packet classification -> Streaming compute -> QDMA subsystem RX -> Network stack
The RecoNIC network flow

- QP and data buffer can be declared either in host or device memory
- RDMA traffic
  - TX path (RDMA write as an example)
    - ➀ Host declares QP, configures RDMA and rings SQ doorbell
    - ➁ RDMA engine fetches WQE from SQ
    - ➂ RDMA engine fetches payload from user buffer and constructs RDMA write packets
    - ➃ RDMA engine sends RDMA write packets
    - ➄ RDMA engine updates CQ when receiving RDMA write acknowledgement packets
    - ❼ Host polls CQ doorbell to detect when RDMA write is done
The RecoNIC network flow

- RDMA traffic
  - RX path (RDMA read response as an example)
    - ➊ Host registers memory region
    - ➋ RDMA engine waits for RDMA read request from a remote peer
    - ➌ RDMA engine validates read requests, fetches payload and constructs RDMA read response packets
    - ➍ RDMA engine sends RDMA read response packets

- Memory region can be declared either in host or device memory
Hardware component: lookaside compute

- Compute acceleration over data stored in device memory
- Datapath interface: AXI4 memory mapped, access data from either device memory or host memory
- Register control interface: AXI4-Lite
- Compute control: two FIFOs
  - Control FIFO: stores user-defined compute control commands
  - Status FIFO: stores completion signals such as kernel ID, job ID, …
- Kernels can trigger RDMA operations
- Potential use cases:
  - Applications required to wait for data from multiple peers before computation
  - Supports HLS and RTL implementations
Hardware component: streaming compute

• Compute acceleration over network data at line-rate
• Datapath interface: AXI4-Streaming
  • Network data
• Control-path interface: AXI4-Lite for internal registers
• Potential use cases
  • Packet processing applications (e.g., packet classification, protocol handling, forwarding, crypto, checksum offloading, security, upper-layer processing, …)
  • Telemetry
  • line-rate application processing such as in-network aggregation
  • …
• Supports Vitis Networking P4, HLS and RTL implementations
RecoNIC software stacks

- **Non-RDMA traffic**: onic-driver
- **RDMA traffic**
  - **Kernel-bypass** RDMA APIs: libreconic
  - **RDMA-core** library (In-progress): reco-provider and reco-ib

**Network stacks**

- **Kernel-bypass RDMA APIs**
  - libreconic
    - `create_rn_dev(...)`
    - `allocate_rdma_qp(...)`
    - `create_a_wqe(...)`
    - `rdma_post_send(...)`
    - `rdma_post_receive(...)`
    - `uint32_t poll_cq_csid(...)`
    - ...

- **RDMA-core**
  - reco-provider
  - reco-ib

- **Non-RDMA traffic**
  - onic-driver

**APIs**

- user-space APIs
- kernel-space driver
RecoNIC software stacks

- Network stacks
- Memory driver
  - Data communication between host and FPGA memory
  - Host as a master
- Control driver
  - Register control
  - Compute control
Built-in lookaside example: network-attached systolic-array MM

- Two peers connected via 100Gbps network
  - data at Peer 1
  - Compute at Peer 2
- Compute control command

```c
typedef struct {
    uint32_t ctl_cmd_size;
    uint32_t a_baseaddr;
    uint32_t b_baseaddr;
    uint32_t c_baseaddr;
    uint16_t a_row;
    uint16_t a_col;
    uint16_t b_col;
    uint16_t work_id;
} ctl_cmd_t;
```

Workflow of the example

1. Initialization and handshaking
2. Constructs a WQE to get data from Peer 1
3. Constructs a WQE to get data from Peer 1
4. Polls CQ doorbells
5. Data is ready
6. Generates and issues a compute control command
7. Waits for compute completion
8. Results are ready
Built-in streaming example: packet classification

- To identify RDMA or non-RDMA traffic
- Designed with Vitis Networking P4
  - Parser
  - Forward
  - De-parser
- Input / output data in AXI4-Streaming
Libfabric over RecoNIC: possible integration

Current software/hardware system

- Applications: ML training/inference, HPC apps, ...
  - User space
  - Kernel space
  - Hardware
  - ReconNIC Shell
  - RDMA-core + reco-provider
  - reco-ib
  - libreconic

Interfacing with libfabric

- Applications: ML training/inference, HPC apps, ...
  - User space
  - Kernel space
  - Hardware
  - ReconNIC Shell
  - RDMA-core + reco-provider
  - reco-ib
  - libreconic
  - libfabric API
  - TCP
  - verbs
  - core

- ReconNIC supports RDMA-core
- RDMA-core provides \textit{libibverbs}, which can be leveraged by the \textit{verbs} provider in libfabric
Data movement performance – Host as a master

- Host as a master to access device memory via QDMA AXI-MM channel
- ~13GB/s for transmitting data >= 512KB
- ~22us for small messages
  - Control overhead

![Bandwidth from host to device memory](image1)

![Latency from host to device memory](image2)
Data movement performance – FPGA as a master

- FPGA as a master to access host memory via PCIe slave bridge
  - Low latency (e.g., 64B)
    - Write (in orange): ~0.17us
    - Read (in blue) : ~0.62us

- Memory access latency over PCIe slave bridge is much faster than that via QDMA AXI-MM channel

- FPGA to access device DDR
  - Low latency (e.g., 64B)
    - Write (in green) : ~0.096us
    - Read (in purple): ~0.196us

- Access latency to device memory is lower than host memory
RDMA read performance

- QP defined in host memory
- Control offloading on FPGA can reduce 22% read latency for small message size (\(\leq 128\)KB)
- Near line-rate throughput for 4KB message
RDMA write performance

- QP defined in host memory
- Control offloading on FPGA can reduce ~29% write latency for small message size (<= 128KB)
- Near line-rate throughput for 8KB message
RDMA latency: host memory vs. device memory

- QP declared in host memory and device memory
- Control offloading on FPGA
- RDMA write latency with QP in device memory is \(~17.32\%\) better than that in host memory
- RDMA read latency with QP in device memory is \(~15.44\%\) better than that in host memory
- DDR access latency is lower than PCIe access latency
RDMA throughput: host memory vs. device memory

- QP declared in host memory and device memory
- Control offloading on FPGA
- RDMA write throughput with QP in device memory is slightly better than that in host memory
- RDMA read throughput with QP in device memory is almost the same with that in host memory, except for 4KB payload size
Conclusion

- RecoNIC is an open-sourced SmartNIC infrastructure/testbed for scale-out computing
  - First SmartNIC platform that interfaces ERNIC with x86 CPUs
  - Provides 100Gb/s line-rate RDMA traffic with low latency
  - Supports streaming and lookaside acceleration via VitisNetP4, HLS or RTL to process network data

- RecoNIC is available at https://github.com/Xilinx/RecoNIC
- A Primer on RecoNIC is available at https://arxiv.org/abs/2312.06207

- If you are interested in RecoNIC, please reach out to Henry (henry.zhong AT amd.com)
References


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